Advances in Fine Pitch Lead Free Assembly Process

Ravi Doraiswami, Sandeep Sankararaman, Woopoung Kim, Jing Li, Zhuqing Zhang, Piyush Gupta, Kensuke Nakanishi*, Manish Borkar, Raghav Madhavan, Vinu Govind, Suna Choi, Ankur O. Aggarwal, Y.Sun, Lianhua Fan, Venky Sundaram, Madhavan Swaminathan, C.P. Wong, Rao R. Tummala

*Harima Chemicals , INC., 671-4 Mizuashi, Noguchi-Cho, Kakogawa, Hyogo, Japan

Packaging Research Center, Georgia Institute of Technology, Atlanta, Georgia 30332
Email: dravi@ee.gatech.edu, Tel: 404-385-0730, Fax: 404-894-3842

Abstract

This research focuses on evolving the best possible criteria for selecting high electrical performance 100 micron pitch lead free solder bumping process. This is achieved through modeling and simulating the pad, process, reliability and test strategy. Coplanar waveguides (CPW) were modeled to evolve process criteria for pad design and choice of materials. Polyimide was chosen as the passivation on the chip. Further signal parasitics were studied for the passivation and a selection criterion was evolved for its thickness. The pad and the passivation layers were studied for dielectric loss when subjected to thermal cycling (air to air). This evaluation leads to the selection of the best pad configuration for lead free solder. An in-depth study on how internal resistance of the solder contributes to the change in parasitics is presented through numerical and simulated models. Standard under bump metallurgy (UBM) was used on the pads. Lead free solder (Sn3.5Ag0.3Cu) was chosen as the bumping material. Bumping strategy was evolved by which solder can be deposited on the UBM without stencil printing or electroplating. Flip chip B-stage underfill was also evaluated for wafer level application and standardized. This paper concludes by suggesting the best design, process and reliability criteria which should be adopted for lead free solder 100 μm pitch flip-chip.

Introduction

IC designers are placing more circuits within a smaller die area, and are pushing the limits of chip performance. Feature sizes both on and off chip are projected to continually decrease[1]. To keep up with such changes packaging techniques also need to improve. Recently the electronics packaging industry has begun to recognize the need for such a requirement. As we go toward smaller dimensions and wafer level packaging, processes become more complicated [2]. Thus controlling process parameters is more difficult and variation in process parameters increases. To gauge the effect of such variations on the electrical characteristics of the chip, the impact of process parameters must be understood. As we move towards wafer level packaging, skin effect is one of the parameters that has a great impact on the bump and is influenced by intermetallics [3, 4]. Electrical characteristics of intermetallics have been studied before, but have focused on resistance measurements only. Their effects on high frequency signals have not been defined.

Wafer level fabrication of chips requires a detailed study of pad, under bump metallurgy (UBM), passivation and wetting. Selection of materials to achieve very good reliability for lead free solder bumping is a challenge. Solder selection is based on the various candidates proposed by NEMI. To achieve fine pitch bumps, it is very important to select the right technique to bump the wafer. Conventional bumping techniques like screen printing and electroplating have their inherent limitations. It is well known that aspect ratios, opening dimensions of the stencil and availability of fine grain solder paste are the limitations for bumping through screen printing [5]. Electroplating ternary lead free solder alloys are costly and have technical problems [6].

The increasing use of flip-chip on organic substrates such as FR-4 printed wiring board (PWB) has relied on underfill to alleviate the thermo-mechanical stress on the solder joints caused by the difference between the coefficient of thermal expansions (CTE) of silicon chip and the organic substrate [7,8]. However, the conventional underfill technology has created many process issues including the slow flow rate, voids, non-homogeneity in the resin/filler system and additional curing time [9]. With the decreasing pitch size down to 100μm, the gap distance becomes so small that the dispensing of the conventional underfill presents great difficulty. On the other hand, the increasing chip dimension also further aggravates the problem. In order to address the problems associated with conventional underfill, wafer level underfill was proposed as a SMT-compatible flip-chip process to achieve low cost and high reliability [10].

In this paper the effect of process conditions on signal parasitics is investigated. Theoretical results for the effect of intermetallics on skin effect for solder and results of a step by step study on the effect of process conditions on signals at each stage of the fabrication of the chip is also presented. Through this extensive study, wafer level packaging design, process and reliability criteria for fabricating 100μm pitch peripheral array chips with lead free solder bumps is presented in detail.

Design

Skin depth is a very important phenomenon at high frequencies. It is the distance from the surface of a metal conductor to the depth at which the magnitude of the penetrating magnetic field falls to a value 1/e of the magnitude at the surface. The mathematical expression for skin depth is:

$$\delta = \frac{1}{\sqrt{\pi \sigma f \mu}} \qquad (1)$$

where,

f = Frequency of the changing magnetic field.

μ = Permeability of the material

σ = Conductivity of the material.

From the above equation, we see that the skin depth becomes larger as resistivity increases and becomes smaller as the frequency and permeability increase. Since the skin depth is larger for metals of poor conductivity, an electromagnetic wave can penetrate more deeply into such metals, allowing some power from the wave to be absorbed into the metal. This power is then dissipated or lost as heat. Hence, ideally, the material should be a perfect conductor so that all the magnetic energy is reflected away; but this is not achievable in practice since all materials have some inherent resistance. We are thus faced with accepting the effects of Maxwell's eddy currents, which are generated in a metal in opposition to the imposed changing magnetic field. These currents dissipate a part of the wave's energy in flowing through the conductor and meeting resistance. If currents flow deeply into a metal of relatively high resistivity, the portion of the conductor in which the flow of current takes place is greater if the frequency of the circuit is relatively low. As the frequency increases, the skin depth is shorter, and eddy currents are then bunched into a decreasing thickness of shell of the conductor, resulting in higher energy loss because of increased current density. This means that a poor conductor can cause serious problems with power loss at high frequencies.

Intermetallics in a bump are initially at the two ends of the bump; near the chip and near the substrate. With the passage of time this intermetallic grows to occupy a greater volume of the bump. Intermetallics have a lower conductivity than pure metal. As described in the previous paragraph, this lower conductivity will result in greater power loss especially at the high frequencies that are in use today.

Here, we study the effect of intermetallic growth on the electrical performance of the bump. Intermetallics are a cause for bump failure. Thus, the bump may be said to fail after a certain number of cycles of duty. This however only describes mechanical failure. Electrically the properties of the bump would have changed dramatically several thermal cycles before mechanical failure due to intermetallic growth, especially in the fine pitch bumps encountered in wafer level packaging. Hence the failure criteria for the bump is no longer accurate because it continues to support one of its prime functions i.e. mechanical support, but has failed electrically.

To study the effect of intermetallics, the different metals that have been investigated are:

1. Silver (Ag)
2. Copper (Cu)
3. Aluminum (Al)
4. Solder
5. Titanium (Ti)
6. Cu_6Sn_5 (Intermetallic)

Data that has been used for these metals is:

A. Conductivities
   a. Silver $= 6.1 \times 10^7$ S/m
   b. Copper $= 5.8 \times 10^7$ S/m
   c. Aluminum $= 3.8 \times 10^7$ S/m
   d. Solder $= 7.0 \times 10^6$ S/m
   e. Titanium $= 2.1 \times 10^6$ S/m
   f. Cu_6Sn_5 $= 5.714286 \times 10^2$ S/m

B. Permeabilities
   a. Silver $= 1.2566 \times 10^{-6}$ H/m
   b. Copper $= 1.2566 \times 10^{-6}$ H/m
   c. Aluminum $= 1.2566 \times 10^{-6}$ H/m
   d. Solder $= 1.2566 \times 10^{-6}$ H/m
   e. Titanium $= 1.2566 \times 10^{-6}$ H/m
   f. Cu_6Sn_5 $= 1.2566 \times 10^{-6}$ H/m

A graph of the skin depths for these metals over a frequency range of 1 GHz to 10 GHz is shown below.

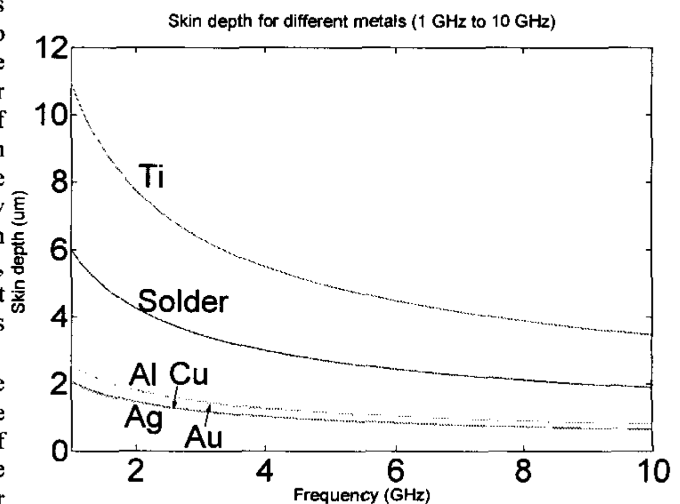

Fig 1: Skin depths of different metals.

As the skin depth of intermetallic is several times larger, the skin depth of intermetallic has been shown in the next figure. For comparison the skin depth of solder is also shown.

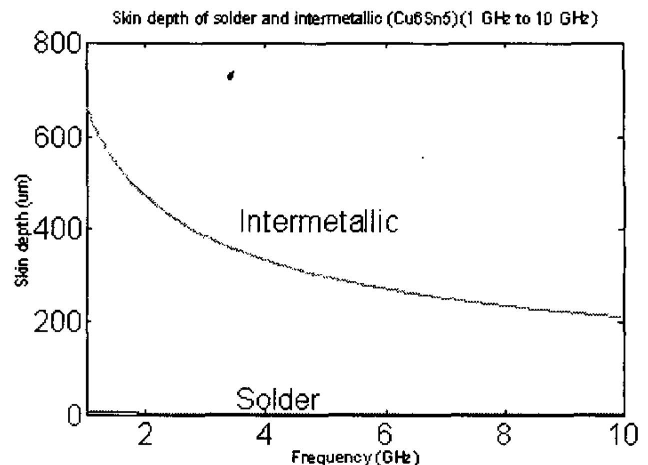

Fig 2: Comparison between skin depths of solder and Cu_6Sn_5.

The resistance of a round wire of radius 'r' is obtained using Johnson's formula. Using this the resistance of a 50μm high column of solder and diameter 50μm as the amount of intermetallic grows is shown in the figure below.

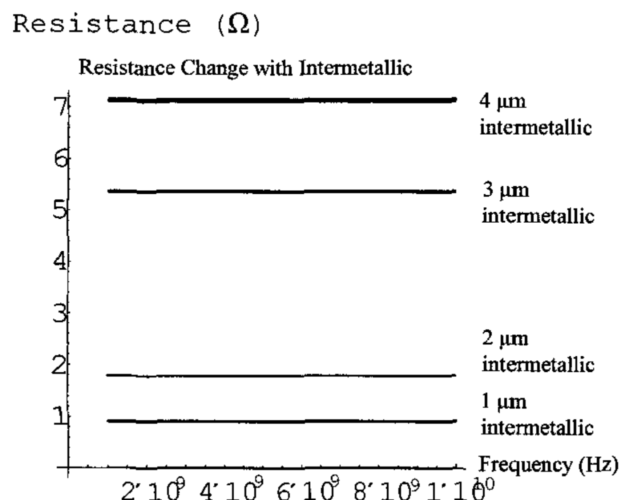

Fig 3: Resistance of solder columns with intermetallics.

The resistance of a pure solder column is so small compared to the resistances of the columns with intermetallics that it is nearly at the X-axis and so cannot be seen in the graph.

It can be seen from Figs.1, 2 and 3 that intermetallics affect the electrical performance in a major way. Hence a study was done on the effect of parasitics at each stage of chip fabrication.

Transmission lines (CPWs), on a silicon substrate, were measured using a Network Analyzer (NA) for extracting the characteristic impedance and propagation constant which include the material properties. Similar to TRL calibration, two lines with the same cross-section and different length were measured. For extracting the propagation constant, the algorithm in [12] was used, which are accurate even with pad parasitics by using the trace of measurement matrices. For the characteristic impedance, it is difficult to find the characteristic impedance using general pad transition models. Therefore, it is restricted to simple pad transition models such as [13] and [14]. In this work, the pad transition model in [13] was used to extract the characteristic impedance. Then, the extracted characteristic impedance (Z_0) and propagation constant (γ) were used for the transmission-line model in Fig. 4 using the following relationships:

$$
\begin{aligned}
R &= \mathrm{Re}\{Z_0 \bullet \gamma\} \\
L &= \mathrm{Im}\{Z_0 \bullet \gamma\}/\omega \\
G &= \mathrm{Re}\{\gamma / Z_0\} \\
C &= \mathrm{Im}\{\gamma / Z_0\}/\omega
\end{aligned}
\qquad (2)
$$

where ω is the angular frequency. The model in Fig. 4 can be simulated using W-elements in HSPICE, which can simulate frequency-dependent RLGC parameters for transmission lines.

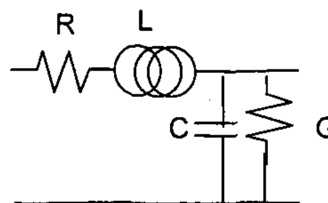

Fig. 4 RLGC models for transmission lines.

Process

The chip size, pads, under bump metallurgy (UBM) and substrate were designed and fabricated using standard clean room wafer level processes. The 100-micron pitch wafer level design consisted of chips having four rows of depopulated peripheral array connections, routed with 2976 I/0's in a 2 cm x 2cm die. A passivation layer to prevent shorting of the connections isolates the different routing arrays. Polyimide was selected as the ideal candidate for passivation that can be photo defined as well as a material that can withstand temperature up to 350°C. The choice of under bump metallurgy is to provide good wetting and bonding with solder and also prevent intermetallic and oxide formation at very high temperatures. Polyimide is spin-coated on the pads. The passivation is pre-baked and openings are made on the pads through photolithography. After photo-defining the passivation layer the wafer went through a final curing process. The wafer was then sent through multiple reflow cycles to test for process reliability. Bumping is performed using eutectic lead solder and lead free solder paste. Fine grain solder paste is printed into the passivation openings and sent through a reflow cycle. The paste grain size was specially tailored to suite the needs for 100μm pitch bumping process shown in Fig. 5.

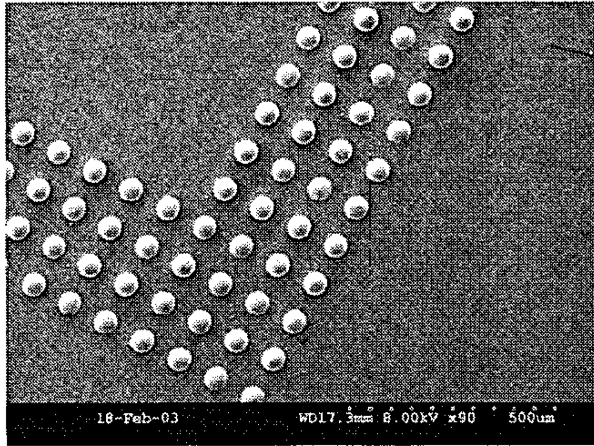

Fig.5 Lead free solder 100 μm pitch bumps (Representing a corner of a periphery array Flip Chip)

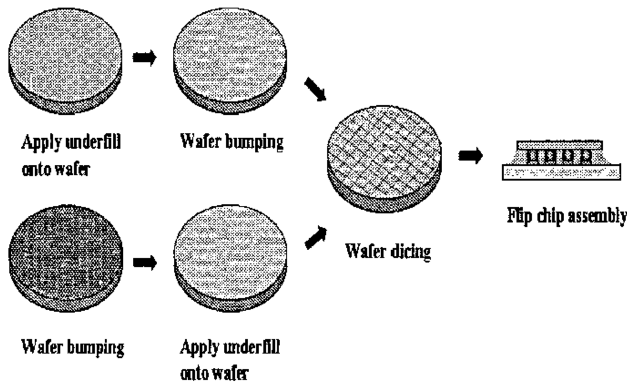

Fig 6. Process Steps of Wafer Level Underfill

Underfill

The B-Stage underfill process steps are illustrated in Fig 6. In this process, the underfill is applied either onto a bumped wafer using a proper method, such as printing or coating or on an unbumped wafer which will be bumped after underfill application. The underfill is usually B-staged before the wafer is diced into single chips. The individual chips are then placed onto the substrate by standard SMT assembly equipment. The underfill is required to possess high curing latency so that the underfill can be flowable at the solder reflow temperature to allow solder wetting on the substrate pads. As the interconnect materials move from SnPb solder to lead-free solder, the reflow temperature is raised by 40~60 °C. This presents great challenges for underfill material design. On the other hand, in order to facilitate dicing, storage and handling, the underfill must appear solid-like and possess enough mechanical integrity and stability after B-stage. Hence, a successful wafer level underfill process requires a fundamental understanding on the underfill curing process, especially the B-stage properties of the underfill.

In this project, a wafer level underfill material was developed and its B-stage properties were characterized. Figure 7 presents the isothermal TGA experiments when the underfill weight was measured as a function of time as the sample was heated to and held at 130 °C. As can be seen in the figure, the drying was almost completed at the first 30 min of isotherm. The underfill material was spin-coated on to a BCB passivated wafer and then heated in the oven at 130 °C for 30 min to remove the solvent and partially cure the underfill. Then the wafer was diced under the normal wafer dicing conditions. Cross-section analysis showed that the underfill thickness was around 60μm. Figure 8 shows the saw street on the wafer. It can be seen that the saw street was relatively clear. The B-staged underfill did not show cracking or delamination under the normal dicing condition.

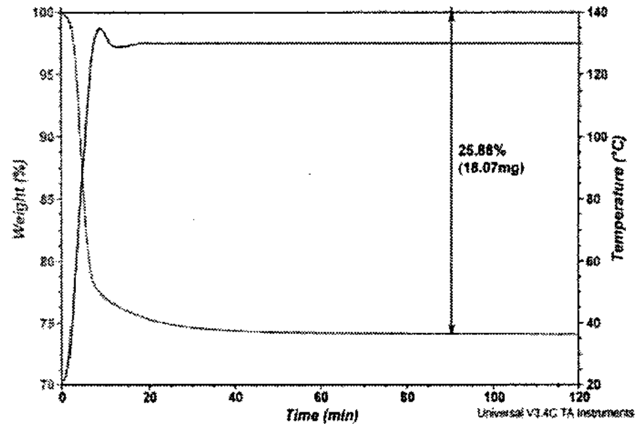

Figure 7. Isothermal TGA study on the underfill B-stage process.

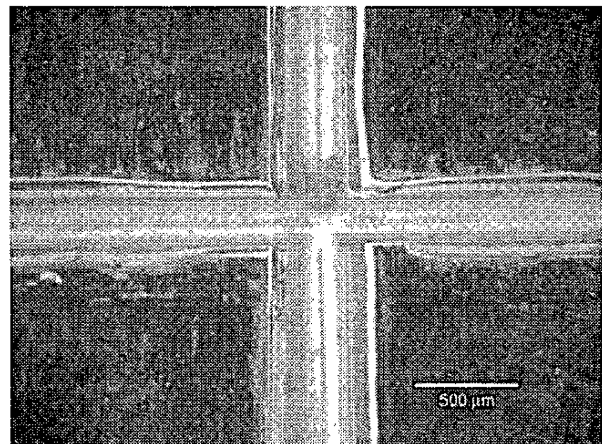

Figure 8. Saw street of the wafer with Underfill

Reliability

Reliability testing was done on a wafer on which coplanar waveguides were fabricated. The change in the electrical characteristics of the waveguide after each test stage was studied as follows. The S-parameters of the line in Fig. 9 were measured using a NA in the frequency range 50 MHz to 10 GHz. The wafer was then placed in a thermal cycling chamber and cycled for 100, 200 and 300 cycles. The S-parameters were measured for the same lines after every 100

cycles. The S-parameters for one of the measured lines are shown in Fig. 10. Polyimide was then coated on an identical wafer and the measurement process repeated on the line shown in Fig 11, which is the same as that in Fig. 9. The coated wafer was also subjected to thermal cycling and the S-parameters were measured after every 100 cycles. The results of the measurement are shown in Fig. 12.

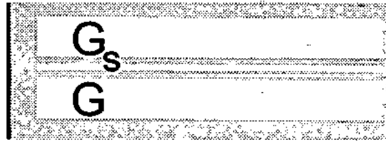

Fig 9: Line on bare wafer.

The results of the measurement are shown below. The Smith Chart (Fig. 10) shows the variation of the S-parameters measured in a NA before and after different stages of thermal cycling. The S_{11} parameter is the input reflection coefficient of 50 Ω terminated output, which serves to indicate the amount of power that is reflected and does not enter the line. The S_{21} parameter is the forward transmission coefficient of 50 Ω terminated output and serves as an indication of the amount of power delivered to the load. In the Smith chart the closer the S_{21} parameter is to the outer circumference the better. As can be seen, the losses in the line increase with thermal cycling reaching a maximum after 100 cycles and then staying the same for 200 and 300 cycles.

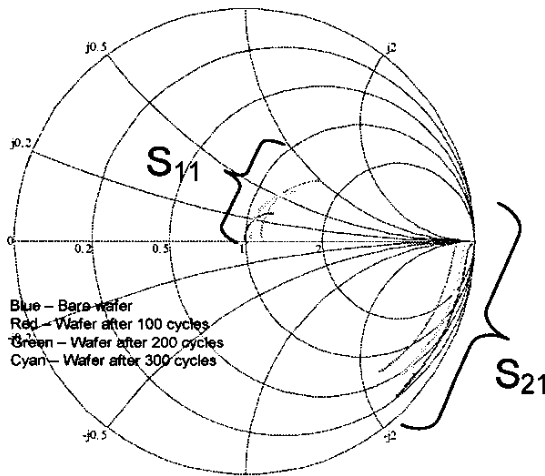

Fig 10: S – Parameter variation with Thermal Cycling for signals between 50 MHz and 10 GHz.

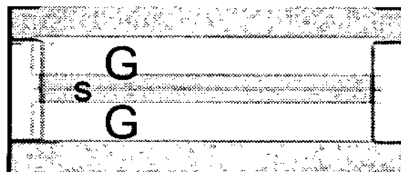

Fig 11: Line on wafer with polyimide.

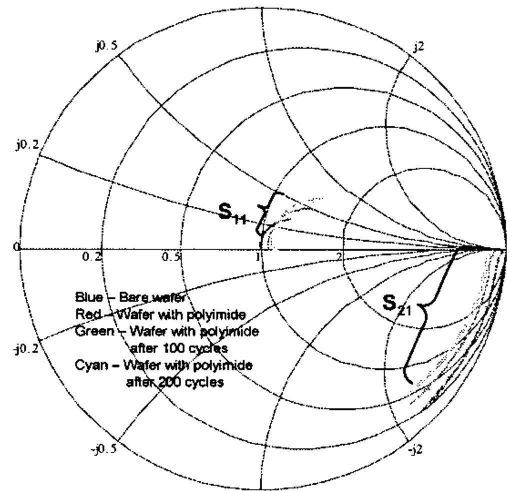

Fig 12: S – Parameter variation with polyimide and thermal cycling for signals between 50 MHz and 10 GHz.

The above Smith Chart shows the variation of the S-parameters measured in a NA before and after different stages of thermal cycling with a polyimide coating on the wafer. As can be seen, the losses in the line increase with thermal cycling. Moreover the losses are higher when compared to the bare wafer when a polyimide coating is present making the electrical properties of polyimide important for high frequencies.

Conclusion

High resistive wafers greater than 2000 Ω-cm were the best selection with 1 micron silicon dioxide layer. Also bumping through paste deposition without the use of stencil or electroplating was achieved, choice of B-Stage underfill was determined and applied for wafer level process. The reliability study showed that parasitics changed when CPW lines were subjected to thermal cycling. Future work is focused on determining what failure modes contribute to various stages in the fabrication process and assembly.

References:

1. ITRS Roadmap 1999.
2. Solberg,V.; Light,D.; Fjelstad,J, "Reliable and Low cost Wafer Level Packaging. Process Description and Qualification Testing Results for Wide Area Vertical Expansion (WAVE ™) Package Technology," Electronics Manufacturing Technology Symposium, 2000. Twenty-Sixth IEEE/CPMT International, 2000, pp. 108 -114
3. Guo-Wei Xiao; Chan, P.C.H.; Teng, A.; Jian Cai; Yuen, M.M.F, "Effect of Cu stud microstructure and electroplating process on intermetallic compounds growth and reliability of flip-chip solder bump," IEEE Transactions on Components, Packaging and Manufacturing Technology, Part A: Packaging

Technologies, Volume: 24 Issue: 4 , Dec 2001, pp. 682 – 690.

4. Frank Stepniak, "Conversion of under bump metallurgy into intermetallics: the impact on flip-chip reliability;" Microelectronics Reliability; vol.41, no.5, May 2001, pp.735-44.
5. Jong-kai Lin, Treliant Fang and Rajiv Bajaj, " Squeegee Bump Technology", Proceedings of the 50th Electronics and component technology conference, 2000 pp 46-53,.
6. Plating technology for electronics packaging, Hideo Honma, Electrochimica Acta, 47, 2001, pp75-84
7. F. Nakano, T. Soga, and S. Amagi, "Resin Insertion Effect on Thermal Cycle Resistivity of Flip-Chip Mounted LSI Devices", Proceedings of International Society of Hybrid Microelectronics Conference, 1987, pp 536.
8. D. Suryanarayana, R. Hsiao, T. P. Gall, and J. M. McCreary, "Flip-Chip Solder Bimp Fatigue Life Enhanced by Polymer Encapsulation", Proceedings of IEEE 40th ECTC, 1990, pp 338.
9. S. Han and K. K. Wang, "Analysis of the Flow of Encapsulant During Underfill Encapsulation of Flip-Chips", IEEE Trans. On CPMT, Part B, Vol. 20(4), 1997, pp 424.
10. S.H. Shi, T. Yamashita, and C.P. Wong, "Development of the Wafer-Level Compressive-Flow Underfill Process and Its Required Materials", Proceedings of the 49th Electronic Components and Technology Conference, 1999, pp. 961.
11. R.B. Marks, "A Multiline Method of Network Analyzer Calibration," IEEE Trans. Microwave Theory and Techniques, vol. 39, Jul. 1991, pp. 1205-1215
12. M. Lee and S. Nam, "An Accurate Broadband Measurement of Substrate Dielectric Constant," IEEE Microwave and Guided Wave Letters., vol. 6, Apr. 1996, pp 168-170 .
13. D. F. Williams, U. Arz, and H.Grabinski, "Accurate Characteristic Impedance Measurement on Silicon," IEEE MTT-Symposium Digest, 1998, pp 1917-1920 .
14. S.Vandengerghe, et al., "Characteristic Impedance Extraction using Calibration Comparison," IEEE Trans. Microwave Theory and Techniques, vol. 49, Dec. 2001, pp 2573-2579.