A 4.5-mW Closed-Loop $\Delta \Sigma$ Micro-Gravity CMOS SOI Accelerometer

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Abstract—In this paper, design, implementation and characterization of a 3-V switched-capacitor (SC) $\Delta \Sigma$ CMOS interface circuit for the closed-loop operation of a lateral capacitive micro-gravity silicon-on-insulator (SOI) accelerometer is presented. The interface circuit is based on a front-end programmable reference-capacitorless SC charge amplifier and a back-end second-order SC $\Delta \Sigma$ modulator. The accelerometer is fabricated through a dry-release high aspect-ratio reduced-gap process. By incorporating the low- $Q$ transfer function of the microaccelerometer in a feedback loop, the system’s dynamic range is improved by 20 dB, leading to a measured resolution of 4 $\mu g/\sqrt{Hz}$ and an output dynamic range of 95 dB at 20 Hz. The bias instability is 2 to 8 $\mu g$ for 12 hours. The chip is fabricated in the 0.5-$\mu$m standard CMOS process with an area of 2.25 mm². The integrated circuit (IC) consumes 4.5 mW of power.

Index Terms—Capacitive interface circuit, Delta-Sigma modulator, force-rebalanced feedback, micro-electromechanical systems (MEMS), micro-gravity accelerometer, quantization noise.

I. INTRODUCTION

THE majority of commercially available MEMS accelerometers have been developed with low to medium range sensitivities suitable for low-cost and high volume applications [1]. In the past few years, there has been an increasing demand for low-power and small form-factor micro-g (g: gravity) accelerometers for a number of applications including inertial measurement units, low-frequency vibration measurements, and earthquake detection [2], [3]. By trading off sensitivity for physical size, ultra-small size high-performance microaccelerometers can be realized (e.g., sub-milli-g resolution in a few square millimeters of area), suitable for large-volume portable applications such as laptops, pocket PCs and cellular phones.

A micro-g accelerometer should preserve high resolution and stability even at the presence of large DC accelerations such as earth gravity. In open-loop systems, the existence of large background accelerations degrades performance and reduces dynamic range [5]. Therefore, closed-loop operation of the accelerometer is essential to improve bandwidth, dynamic range and linearity [6]–[13]. We had previously reported an open-loop first-order $\Delta \Sigma$ CMOS SOI capacitive microaccelerometer with a resolution of 110 $\mu g$/Hz and sensitivity of 0.2 pF/g [4], [22]. In this work, through innovation in sensor process technology and IC design, we present a force-rebalanced SOI accelerometer, employing a low-power second-order electrical $\Delta \Sigma$ modulator with micro-g resolution and stability, and an extended dynamic range of 95 dB. A 22 dB improvement in noise and dynamic range is achieved with a sampling clock of 40 kHz corresponding to a low oversampling ratio (OSR) of 40. Fig. 1 shows the schematic diagram of the improved SOI accelerometer. The movement of the seismic proof mass causes the inter-electrode capacitors to change, and the interface circuit detects minute changes of the sensor’s capacitance in a fully differential configuration.

In contrast to the previously reported closed-loop $\Delta \Sigma$ microaccelerometers, in which the high- $Q$ mechanical transfer function of the sensor was typically the only element of the loop-filter [8]–[10], in our design, a second-order $\Delta \Sigma$ modulator is cascaded with the high-sensitivity low- $Q$ accelerometer and the front-end charge amplifier. Therefore, the closed-loop system is inherently stable, and there is no need for digital compensation [12]. The accelerometer’s transfer function improves the reduction of in-band quantization and electronic noises. In addition, there is not a distinct feedback clock phase involved in our architecture, which reduces the complexity of the system [11]. In other words, two comb-drive actuators are continuously applying the appropriate feedback force to the proof mass, and the output bitstream controls the average of the applied feedback force [9], [13]. Accelerometers are fabricated in low-resistivity ($< 0.01 \Omega cm$) 120-$\mu$m-thick SOI substrates with added solid mass and reduced capacitive gaps, using a high-yield dry-release MEMS process [2], [14]. In this implementation, the sensor’s sensitivity ($\Delta C/\text{gravity}$) is increased by capacitive gap reduction through post-deposition of doped low-pressure chemical-vapor-deposited (LPCVD) polysilicon. The mechanical noise floor is also improved by increasing the solid seismic mass by saving parts of the thick handle layer under the proof mass. Accelerometers are designed for a Brownian noise equivalent acceleration (BNEA) of 1 $\mu g/\sqrt{Hz}$. The measured output noise of the front-end IC shows a circuit noise equivalent acceleration (CNEA) of better than 1 $\mu g/\sqrt{Hz}$. The measured total noise equivalent acceleration (TNEA) for the combined accelerometer and IC is 4 $\mu g/\sqrt{Hz}$ at 20 Hz; this is slightly higher than expected, which is attributed to nonidealities in MEMS fabrication, imposing higher damping and higher BNEA. High capacitive sensitivity of the accelerometer eliminates high gain requirement for the front-end amplifier and improves the baseband quantization noise filtration [7]. Fig. 2 illustrates the simplified schematic of the accelerometer showing the electrode configuration.

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The accelerometer operates in air and is designed for non-peaking (low-\(Q\)) response with a bandwidth of 500 Hz [2], [15]. Dynamic behavior of the sensor is governed by Newton’s second law of motion. The sense capacitance is split into four identical sub-capacitances in a fully symmetric and differential manner (two increasing and two decreasing). The accelerometer is wire-bonded to the IC chip. The interface IC is implemented in a standard 3-V 0.5-\(\mu\)m N-well CMOS process. The IC’s output bitstream is buffered and fed back to the accelerometer through a set of comb-drive actuators. The main advantage of using comb-drive feedback (compared to parallel-plate actuator) is that the electrostatic feedback force does not depend on the proof mass displacement and is independent of the comb electrodes’ overlap, which provides linearity [6]–[9]. Since comb-drive electrodes are implemented in thick SOI wafer with reduced gap, the generated electrostatic force is strong enough to null the movement of the proof mass. At the entrance gate of the front-end IC, an input switching scheme is devised such that the charge amplifier can interface with four changing capacitances of the sensor, having one common node at the proof mass [16]. This architecture provides a better versatility in accommodating different capacitive sensors. Other capacitive interface architectures typically employ two changing capacitors with a common node, requiring area-consuming on-chip reference capacitors to form a balanced capacitive bridge and set the input common mode voltage of the amplifier [4], [11], [17], [18].

This paper is organized as follows. Section II introduces the functional block diagram of an electromechanical \(\Delta\Sigma\) microaccelerometer and its principle of operation. Section III presents an overview of the accelerometer design and fabrication. Section IV provides the closed-loop circuit design and implementation, including front-end and back-end blocks. Section V demonstrates the MEMS-IC measured performance results. The conclusion is provided in Section VI.

II. ELECTROMECHANICAL \(\Delta\Sigma\) MICROACCELEROMETER

The functional block diagram of a closed-loop capacitive microaccelerometer system is shown in Fig. 3.

The accelerometer consists of a seismic proof mass with parallel-plate sense capacitors \(C_{S1}, C_{S2}, C_{R1}\), and \(C_{R2}\) and comb-drive actuators \(C_{C1}\), and \(C_{C2}\). For small proof mass displacement, the differential sense capacitance is defined as

\[
\Delta C_S \cong \frac{n_P \varepsilon_0 d_P h}{2d_P^2} x = \frac{C_S}{d_P^2} x
\]  

where \(n_P\) is the total number of parallel-plate sense electrodes with length of \(l_P\), and initial gap spacing of \(d_P\); \(x\) is the proof mass displacement from the rest position; \(C_S\) is the half of the rest capacitance in between the proof mass and sense fingers. In a force-rebalanced capacitive accelerometer, the error force \(F_{ERR}\) between the external force \(F_{EXT}\) and the feedback force \(F_{ELC}\) passes through the mechanical transfer function...
of the accelerometer that has a second-order response with respect to the proof mass displacement. The seismic mass displacement is eventually converted to the capacitance changes.

$$G_{AXL}(s) = \frac{\Delta C_s(s)}{F_{ERR}(s)} = \frac{G_{AXL_0}}{\left(\frac{s}{\omega_0}\right)^2 + \frac{1}{Q} \left(\frac{s}{\omega_0}\right) + 1}$$  \hspace{1cm} (2)$$

and

$$G_{AXL_0} = \frac{1}{K} \frac{C_s}{d_p} \omega_0 = \sqrt{\frac{K}{M'}} Q = \sqrt{\frac{KM}{D}}$$  \hspace{1cm} (3)$$

where $M$ is the mass, $K$ is the effective stiffness, $D$ is the air damping, and $\omega_0$ is the natural angular frequency. To make control design parameters more tolerant to parameter variations of the mechanical sensor and avoid instability, the accelerometer operates in air and has an over-damped response. The front-end noninverting SC charge amplifier, with a programmable amplification capacitor of $C_A$, picks up the sensor capacitive changes and provides an amplified voltage proportional to the input force [16]. The system transfer function is defined as the ratio of the front-end differential output voltage over the input force.

$$G_{TDR}(s) = \frac{V_i(s)}{F_{ERR}(s)} = \frac{G_{TDR_0}}{\left(\frac{s}{\omega_0}\right)^2 + \frac{1}{Q} \left(\frac{s}{\omega_0}\right) + 1}$$  \hspace{1cm} (4)$$

where

$$G_{TDR_0} = G_{AXL_0} G_{AMP}$$  \hspace{1cm} (5)$$

$$G_{AMP} = \frac{V_{DD}}{C_A}. \hspace{1cm} (6)$$

The converted front-end output is digitized by the back-end second-order $\Delta \Sigma$ modulator with a 1-bit output stream. Fig. 4 shows the $z$-domain linear model of a second-order $\Delta \Sigma$ modulator with unity-gain integrators [19].

The output signal is equal to

$$Y(z) = G_{AMP} z^{-1} \Delta C_s(z) + G_{AMP} z^{-1} N(z) + z^{-1} (1 - z^{-1}) P(z) + (1 - z^{-1})^2 Q(z). \hspace{1cm} (7)$$

As expected, the quantization noise, $Q(z)$, is up-converted through a second-order high-pass filter. Also, the input referred noise of the second integrator, $P(z)$, is improved through a first-order high-pass filter. However, the input referred noise of the amplifier, $N(z)$, is still a dominating noise source that degrades the in-band signal-to-noise ratio (SNR). To close the electromechanical loop, the 1-bit output stream is fed back to the comb-drive actuator from which generates an electrostatic force ($F_C$) to push the proof mass back to the null position.

$$F_C = \frac{V_{FB}^2}{2} \frac{\partial C_C}{\partial x} = \frac{n_C \omega_0 h V_{FB}^2}{4 d_C} \hspace{1cm} (8)$$

In this equation, $V_{FB}$ is the feedback voltage; $n_C$ is the number of comb-drives; $d_C$ is the gap size in comb-drives. Although the electrostatic force is displacement-independent but it is still proportional to the square of the applied feedback voltage $V_{FB}$, which is represented as a nonlinear convolution transformation in the frequency domain. However, the convolution of two identical square waves is equal to the same square wave with squared pulse amplitude, presented as a constant gain in the feedback path. Since the switched-capacitor (SC) charge amplifier is a sampled-data system with a sampling period of $T_S$, it is required to find the step-invariant or zero-order-hold (ZOH) transform of $G_{TDR}(s)$ [20], [21].

$$G_{TRD}(z) = \frac{G_{TDR_0}(A_1 z + A_0)}{z^2 - B_1 z + B_0}$$  \hspace{1cm} (9)$$

where

$$A_1 = 1 - e^{-a T_S} \cos b T_S - \frac{a}{b} e^{-a T_S} \sin b T_S$$  \hspace{1cm} (10)$$

$$A_0 = e^{-2a T_S} - e^{-a T_S} \cos b T_S + \frac{a}{b} e^{-a T_S} \sin b T_S$$  \hspace{1cm} (11)$$

$$B_1 = 2e^{-a T_S} \cos b T_S$$  \hspace{1cm} (12)$$

$$B_0 = e^{-a T_S}$$  \hspace{1cm} (13)$$

$$a = \frac{\omega_0}{2Q}$$  \hspace{1cm} (14)$$

$$b^2 = \omega_0^2 \left(1 - \frac{1}{4Q^2}\right). \hspace{1cm} (15)$$

In light of the above discussion, the entire force-rebalanced microaccelerometer system is illustrated in Fig. 5. The signal transfer function (STF), noise transfer function (NTF), and quantization noise transfer function (QTF) are calculated as below:

$$STF(z) = \frac{Y(z)}{F_{EXT}(z)} = \frac{G_{TDR_0}(A_1 z + A_0) z^{-1}}{z^2 - B_1 z + B_0} \frac{1}{1 + G_{ACT} G_{TDR_0}(A_1 z + A_0) z^{-1}} \hspace{1cm} (16)$$

$$NTF(z) = \frac{Y(z)}{F_{EXT}(z)} = \frac{G_{AMP} z^{-1}}{1 + G_{ACT} G_{TDR_0}(A_1 z + A_0) z^{-1}} \hspace{1cm} (17)$$

$$QTF(z) = \frac{Y(z)}{Q(z)} = \frac{(1 - z^{-1})^2}{1 + G_{ACT} G_{TDR_0}(A_1 z + A_0) z^{-1}} \hspace{1cm} (18)$$

Equations (17) and (18) show that the input referred noise and the quantization noise are further attenuated by the overall loop gain of $(G_{ACT} G_{AMP} G_{AXL_0}(A_1 + A_0))/(1 - B_1 + B_0)$.
Fig. 5. \(z\)-domain model of the proposed force-rebalanced \(\Delta\Sigma\) microaccelerometer.

Fig. 6. Simulated frequency response of the quantization noise transfer function, illustrating 20 dB extra noise reduction for the closed-loop system.

at very low frequencies (so-called baseband), as shown in the plotted response of QTF in Fig. 6.

III. HIGH-PERFORMANCE SOI MICROACCELEROMETERS

In this work, the resolution and sensitivity of the dry-released SOI accelerometers are each improved by 25 \(\times\) compared to [22] to achieve sub-10 \(\mu g/\sqrt{Hz}\) resolution and stability in a small form-factor \((<0.4 \text{ cm}^2)\) [23]. The figure of merit, defined as the ratio of the device sensitivity to its mechanical noise floor, is improved by increasing the solid seismic mass and reducing capacitive gaps. Fig. 7 illustrates the two-mask fabrication process flow of the micro-g SOI accelerometer. A detailed description of the fabrication process is provided in [2] and [14]. Scanning electron microscopy (SEM) pictures of a prototype device are shown in Fig. 8. Fig. 8(b) shows a close-up view of the electrodes and shock absorbers. The gap reduction technique relaxes the aspect-ratio of the trench etching process [24] and allows for different gap sizes to implement shock stops or provide comb-drive actuators with smaller gaps in thick SOI wafers. This feature is not available in processes that are based on sacrificial layer gap definition [9], [15].

A. Accelerometer Design Process

The Brownian noise equivalent acceleration (BNEA) of the suspended mass is the fundamental resolution limit. This acceleration is expressed as [25], [26]

\[
BNEA = \frac{\sqrt{k_B T D}}{M}. \tag{19}
\]

In this equation, \(k_B\) is the Boltzmann constant, \(T\) is the absolute temperature, \(D\) is the air damping, and \(M\) is the seismic mass. Increasing the mass and reducing the damping improves BNEA. However, reducing the damping increases the instability of the accelerometer, which is not desirable. Another limiting factor is the circuit noise equivalent acceleration (CNEA) that depends on the capacitive resolution of the interface circuit \((\Delta C_{\text{MIN}})\) and the capacitive sensitivity \((S)\) of the accelerometer \((S = \Delta C/\text{gravity})\):

\[
CNEA = \frac{\Delta C_{\text{MIN}}}{S}. \tag{20}
\]

Finally, the total noise equivalent acceleration (TNEA) of the accelerometer is expressed as

\[
TNEA = \sqrt{BNEA^2 + CNEA^2}. \tag{21}
\]

The design objective is the minimization of the BNEA and optimization of device sensitivity while preserving process sim-
Table I shows the design specifications of the capacitive SOI accelerometer.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proof mass size</td>
<td>3 mm × 5 mm</td>
</tr>
<tr>
<td>Overall sensor size</td>
<td>6 mm × 6 mm</td>
</tr>
<tr>
<td>Device thickness</td>
<td>120 μm</td>
</tr>
<tr>
<td>Sense gap</td>
<td>4 μm</td>
</tr>
<tr>
<td>Proof mass (M)</td>
<td>5 milli-gram</td>
</tr>
<tr>
<td>Quality factor (Q)</td>
<td>0.3</td>
</tr>
<tr>
<td>BNEA</td>
<td>1 μg/Hz</td>
</tr>
<tr>
<td>Static sensitivity (S)</td>
<td>5 pF/g</td>
</tr>
</tbody>
</table>

Fig. 8. SEM pictures of a prototype SOI accelerometer.

IV. CLOSED-LOOP INTERFACE ARCHITECTURE

Fig. 9 illustrates the overall block diagram of the implemented closed-loop ΔΣ microaccelerometer system. The interface IC relies on a fully differential input/output front-end–back-end architecture. The front-end includes a reference-capacitorless SC charge amplifier with a 3-bit programmable gain (Fig. 10) [16]. The back-end is composed of two cascaded SC integrators with programmable gain of 0.5 or 1, a two-level quantizer and feedback network. To reduce the effect of the opamp offset and low-frequency noises, the correlated double-sampling (CDS) scheme is used [4]. The core opamp in each block is a low-power low-noise fully differential folded-regulated cascode operational transconductance amplifier (OTA) with a very high DC gain of approximately 90 dB that improves the SC functionality and noise performance (Fig. 11) [27]. The output common-mode feedback (CMFB) includes a buffered resistor-averaged circuit and a common-mode error amplifier that makes it possible to test the OTA block separately. The OTA can provide a differential output swing of 4 V from a single supply of 3 V. The interface circuit is designed for a lower power consumption compared to [4] and therefore, lower OSR is used. However, by using a second-order electrical ΔΣ modulator with the sensor transfer function in the loop, an effective output dynamic range of 95 dB is achieved at 20 Hz. SOI accelerometers are wire-bonded to the front-end IC and are tested for static and dynamic responses.

A. Back-End Second-Order SC ΔΣ Modulator

The schematic diagram of the back-end ΔΣ modulator is shown in Fig. 12. The 1-bit quantizer is composed of a comparator and a transmission gate (TG) D-latch flip-flop. The digital output is latched at the falling edge of φ2, which is the moment to make the decision about the output of 1-bit DAC. Using an appropriate combination of inverting and noninverting SC building blocks, the required delays in the z-domain model of the ΔΣ modulator are generated. For example, a noninverting SC integrator inherently generates a half-delay while an inverting SC integrator imposes no delay on the signal pass. Integrating capacitances (C1 and C2) interpolate subsequent sampled data and provide an integrated analog output. The comparator’s output bitstream is externally buffered and fed back to the accelerometer’s comb actuator to push the proof mass to the null position. The chip microphotograph of the entire front-end–back-end interface IC is shown in Fig. 13. Different blocks are labeled on the picture. The IC chip measures a silicon area of 2.25 mm² and consumes a low power of 4.5 mW with a sampling clock of 40 kHz.
Fig. 10. Schematic diagram of the reference-capacitorless SC front-end circuit [16].

Fig. 11. Schematic diagram of a gain boosted folded-cascode OTA.

Fig. 12. Schematic diagram of the back-end modulator.
Fig. 13. Chip microphotograph.

Fig. 14. Custom-designed PCB to test the ΔΣ CMOS SOI accelerometer.

V. CMOS MEMS Interface Test Results

A prototype SOI accelerometer is wire-bonded to the IC chip and is tested for the open-loop and closed-loop static and dynamic operations. Fig. 14 shows the picture of a custom-designed printed circuit board (PCB) to test the system. The accelerometer has a measured sensitivity of 5 pF/g, equivalent to a system gain of 30 V/g. Fig. 15 shows the open-loop and closed-loop response of the system to DC and AC (50 milli-g peak at 0.6 Hz) accelerations.

In this figure, CH1 shows the 1-bit output bitstream and CH2 shows the charge amplifier’s output (error signal). In the open-loop system, the error signal is large since the proof mass displacement is substantial. In the closed-loop configuration, the output bitstream is applied to the comb-drive electrodes. The actuator’s electrostatic force imposes a negative feedback to push back the proof mass, hence the error signal reduces significantly.

Fig. 16 shows the ΔΣ modulators’ output power spectrum, illustrating the in-band noise shaping and the up-conversion of the quantization noise. In this case, the output bit stream was connected to a spectrum analyzer through an active probe, to avoid 50 Ω loading effect. There are no in-band tones at the output spectrum, which means the closed-loop system is functional for the input bandwidth of 500 Hz. The closed-loop system provides a noise reduction of 22 dB, corresponding to an output dynamic range of 95 dB and a resolution of 15 bits at 20 Hz. The CMOS SOI accelerometer is tested for the bias instability over 12 hours in a laboratory environment. Fig. 17 shows the bias instability of the accelerometer system that is extracted from measured zero acceleration output using the Allan Variance analysis [28]. In this figure, the inset plots show the measured acceleration through the front-end in a time period of 12 hours in a lab environment. In Fig. 17(a), the dashed line corresponds to very-low frequency components of the acceleration at the output of the SC charge amplifier, which are caused by the temperature change or environmental interferences. The closed-loop system shows a significant improvement in the bias instability at extremely low frequencies compared to the open-loop configuration [Fig. 17(b)]. The closed-loop bias instability is in the range of 2–8 μg. Table II shows the measured specifications of the force-rebalanced micro-gravity ΔΣ CMOS SOI accelerometer.
The measured resolution is 4 µg at 20 Hz, which is dominated by the BNEA.

<table>
<thead>
<tr>
<th>TABLE II</th>
<th>MEASURED PERFORMANCE OF THE CLOSED-LOOP ΔΣ SOI ACCELEROMETER</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input bandwidth</td>
<td>500 Hz</td>
</tr>
<tr>
<td>Front-end gain</td>
<td>30 V/g (C₀=0.5 pF)</td>
</tr>
<tr>
<td>Output noise</td>
<td>-87 dBV/√Hz @ 20 Hz</td>
</tr>
<tr>
<td>TNEA</td>
<td>4 µg/√Hz @ 20 Hz</td>
</tr>
<tr>
<td>Capacitive resolution</td>
<td>2 aF/√Hz @ 20 Hz</td>
</tr>
<tr>
<td>Bias instability</td>
<td>2-8 µg (for 12 hours)</td>
</tr>
<tr>
<td>Dynamic range</td>
<td>95 dB (15 bits of resolution)</td>
</tr>
<tr>
<td>Sampling clock</td>
<td>40 kHz</td>
</tr>
<tr>
<td>OSR</td>
<td>40</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>4.5 mW (3V-GND)</td>
</tr>
<tr>
<td>Chip area</td>
<td>2.25 mm²</td>
</tr>
</tbody>
</table>

VI. CONCLUSION

The implementation and characterization of a force-rebalanced ΔΣ CMOS SOI accelerometer with micro-gravity resolution and stability was presented. A reference-capacitorless front-end IC was designed and implemented that has the ability of interfacing capacitive sensors with large rest capacitors including bulk-micromachined accelerometers. It eliminates area-consuming on-chip reference capacitors and increases the versatility of the front-end block. In this architecture, the proof mass is tied to a constant voltage source (0.5 V_DD) at all times and never switched. This in turn simplifies the digital clock generator and reduces the charge injection noise. The accelerometer was fabricated in low-resistivity (< 0.01 Ω·cm) 120-µm-thick SOI substrates with reduced capacitive gaps using a high-yield dry-release fabrication process. By incorporating sensor’s transfer function in the closed-loop system, a 22 dB improvement in noise and dynamic range was achieved with a sampling clock of 40 kHz corresponding to a low oversampling ratio of 40. The interface IC draws 1.5 mA from a 3-V supply.
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