Precise Release and Insulation Technology for Vertical Hall Sensors and Trench-Defined MEMS

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Abstract
Vertical Hall sensors have been fabricated using a new process combining deep-RIE silicon trench etching and anisotropic TMAH silicon wet etching to precisely define the sensor’s active area. The demonstrated release of the bottom of the devices with a wet etching step results in a well-defined and uniformly doped active area. The trench-defined vertical Hall sensors show a very high current related sensitivity of up to 1000 V/AT, a non-linearity of 0.06 %FSO, and a residual offset (after spinning current offset reduction) of about 0.5 mT. A method for etching the polysilicon inside the trenches using XeF$_2$ without additional mask is demonstrated on an SOI wafer. While the technology is demonstrated for vertical Hall sensors, it is also well suited for the fabrication and release of trench-defined MEMS, such as thin beams.

Keyword
Vertical Hall Sensor, TMAH, XeF$_2$, DRIE trench etching.

INTRODUCTION
The input-equivalent magnetic field offset voltage is generally considered to be the limiting figure of merit of Hall sensors. Spinning current methods are efficient ways of compensating the initial offset voltages. They theoretically lead to a total offset cancellation for linear devices (i.e. the contact currents are a linear combination of the contact voltages) of any shape. However, it’s practically very difficult to build linear sensors, since conventional lateral Hall plates as well as vertical Hall sensors (VHS) usually make use of a diode as insulation technique. The geometrical symmetry of the spinning phases can counterbalance the lack of linearity of the devices. Nevertheless, any imperfection or perturbing effects (e.g. the piezoresistive effect), that would cancel out in the linear case, will then generate a non-compensated offset. Since lateral Hall plates benefit from a higher symmetry order, as well as a better geometrical control compared to the VHS, they exhibit a better spinning current efficiency. Previous VHS have been insulated from the bulk either sidewise by deep-RIE trenches and on the bottom by a pn-junction or by pn-junctions only [1-2]. In this work, a new technology for eliminating the bottom diode of the trench insulated VHS is presented. Moreover a method for etching the polysilicon inside the trenches using XeF$_2$ without additional mask has been developed and is demonstrated on an SOI wafer. This etching reduces the stress on the device, and increases the sensor linearity by decreasing the field effect generated by the bulk on the active area.

DESIGN CONSIDERATIONS
The goal is to develop a fabrication process that can later be used as a single-mask preprocessing sequence followed by a standard industrial CMOS process, as presented in [3]. Only the optional XeF$_2$ etching step is to be done after completion of the CMOS process. In this work however, the process “back-end” (contacts and metallization) has been performed in house and required two additional masks. A typical sensor layout is shown in Figure 1:

![Figure 1: Typical sensor layout.](image)

The thickness of the active area is reduced to the minimum (about 2 microns) in order to maximize the sensor’s current related sensitivity. Throughout the release of the sensor bottom, the active area has to be hold in place. Anchoring pillars have been preferred to a direct fixture to the bulk for the following reason. During the active area implantation, the sidewalls of the bulk are also implanted. Therefore the trenches have to completely enclose the active area, to prevent part of the bias current between two contacts to flow through the bulk. The polysilicon refilling the trenches can optionally be etched. For the purpose of limiting the number of masks and process steps, the openings used for this etching are structured in parallel to the contact openings, but remain uncovered by the metal. The openings have been placed rather far from the active area so that a small misalignment does not cause the etching of the active sensor area.

FABRICATION PROCESS
Process steps
The process (see Figure 2) starts with the thermal oxidation of the p-type silicon wafer. The generated oxide is used as mask for: the trench etching, the silicon sidewall implant, as
As well as the bottom release of the active area. The masking oxide is patterned with an ICP etching system using a CF$_4$/H$_2$ chemistry and the 20 microns deep silicon trenches are etched by means of the Bosch process (low frequency on the SOI wafers for avoiding the notching effect). Next, the trench-sidewalls are implanted with high-energy phosphorus in a tilted quad-mod setup. The wafers are then coated with a thin conformal high-temperature oxide layer (preferred to thermal oxide, to prevent the immobilization of the dopants), that electrically insulates the walls of the sensor active area. In a subsequent anisotropic dry etching step, the oxide is removed at the bottom of the trenches. A few additional Bosch process cycles are now required to define the following wet-etch boundaries. Afterwards, the wafers are immersed in TMAH, thus releasing the bottom of the active area. The exposed silicon surfaces on the bottom of the trenches are insulated with an oxide layer, and the trenches are refilled with polysilicon to enable electrical connections to the sensor contacts. A conformal LPCVD process is used to deposit the polysilicon. If the polysilicon should act as a shield, the process can be performed in two steps with an intermediate doping. The polysilicon at the wafer surface is then blanket-etched in an ICP-machine, and the underlying top oxide is removed in BOE. Afterwards, a field oxide is thermally grown on the wafer. This step is also used as drive-in for the dopants in the active area. After being patterned, the contacts are implanted with As through a thin oxide to create shallow n+ regions.

Following the dopant activation, Al with 1%Si is sputtered and patterned to form the electrical connections to the sensor. As a last step, the polysilicon in the trenches may be etched in a XeF$_2$ reactor. XeF$_2$ is able to etch the polysilicon in the trenches up to a depth of 20 microns and with an excellent selectivity of more than 100:1 over the oxide and the aluminum.

**Results and discussion**

**Preprocessing**

Figure 3 shows a cross section of the sensor. The TMAH wet etching has very precisely shaped the bottom of the sensor active area (bound by two intersecting <111> planes). The lower right corner of the bulk opening did not benefit of the anisotropic etch stop because of the convex corners in the pillar region (circled region in Figure 3 (b)).

![Figure 3](image)

Compared to similar release methods such as SCREAM [1], the developed CMOS-compatible technology provides better dimensional control. Moreover, since the etch stop of the TMAH etching is geometry rather than time defined, the process is less sensitive to over-etching and non-uniformity.
issues on device- as well as wafer-level. Note that doing a strong overetch with the bent active area design of Figure 3 (b), would lead to an oblique bottom surface of the device, due to the convex edges in the corners. A schematic of the edges of the region enclosed by the trenches as seen from the plane indicated in Figure 2 (f) is shown in Figure 4.

**Figure 4: Schematic of the edges of the region enclosed by the trenches as seen from the plane indicated in Figure 2 (f).**

**Postprocessing**

The XeF$_2$ polysilicon etching has been performed on SOI devices (i.e. instead of a wet etching, a buried oxide has been used for the bottom insulation). Figure 5 shows a cross-section and a top view of the etched devices. The polysilicon has been fully etched inside the trenches, and as expected, none of the monocrystalline silicon parts protected by the sidewall oxide has been attacked. The scallops of the Bosch-process can be distinguished on the columns on each side of the active area. The refinements that can be observed at the base of the trenches are due to the low frequency Bosch-process performed at the end of the trench etching to avoid notching effects.

![Cross-section and top view of etched devices](image)

**Figure 5: (a) Cross-section and (b) top view of VHS on SOI wafer with the polysilicon inside the trenches etched by XeF$_2$.**

The Bosch-process automatically stops on the buried oxide of the SOI substrate. However, the trench floor lies a bit higher because of the 0.3-microns thick high temperature oxide that is also deposited on the bottom of the trenches. The kind of stalactites sometimes broken that can be seen in Figure 5 (b) are constituted by oxidized polysilicon. These appear in the trench crossings. Due to the extreme conformality of the polysilicon, cylindrical holes remains in the center of the crossings, and enable the polysilicon oxidation.

**DEVICES MEASUREMENTS**

**Electric measurements**

Prior to the magnetic measurements, the device insulation and contacts have been tested. To this end, a V-I curve is measured between the bulk and all the sensor contacts together. The measurement has to be performed in the dark, to avoid the production of a generation photocurrent in the reverse biased diode depletion layer.

![Bulk-contacts current vs. voltage curve](image)

**Figure 6: Bulk-contacts current vs. voltage curve.**

Figure 6 shows a typical measured pn-junction charasteristic. This is expected since the anchoring pillars holding the sensor active area are diode insulated from the bulk substrate. This junction however can easily be positioned far away from the active area.

The V-I characteristics measured between the two external contacts of four-contact devices on SOI substrates are plotted in Figure 7 as a function of the carrier/device layer potential.

![Contact-contacts current vs. voltage curve](image)

**Figure 7: V-I Characteristics between the outer contacts of 4-contact devices for XeF2 etched (dotted line) and non-etched (plain line) VHS on SOI with the bulk voltage as parameter. One of the contacts is maintained at 0V.**
The V-I characteristic of the non-etched sensor strongly depend on the bulk voltage and are less linear than the ones of the etched device. That can be explained considering the field effect created by the bulk on the active area. The sensor acts similarly to a normally on MOS transistor, the channel of which being the active area, the bulk being the gate, and the two contacts being the source and drain. The measured curves indeed resemble the Ids vs Vds behavior of a MOS transistor. Since the dielectric constant of air is one order of magnitude lower than the one of polysilicon, the bulk voltage influences much less the etched device. The remaining non-linearities of the etched sensor may stemm from the field effect generated by the bottom boundary, and from the contact characteristics that aren’t perfectly linear themselves.

As mentionned earlier, a linear behaviour is required for an efficient spinning current offset cancellation. Reducing the field effect implies to decrease the charge on the MOS capacitor. This can be achieved by reducing the capacitance value, or the voltage across it. The surface cannot be modified, and wider trenches would necessitate a longer polysilicon deposition, which is an expensive and time consuming process. The most efficient way to decrease the capacitance remains the etching of the polysilicon, that is anyway beneficial from the stress point of view. In the purpose of decreasing the voltage between the bulk and the active area, contact arrays can be added in the bulk n-type region on each side of the device. The potential distribution in the active area can then be mirrored in the bulk using voltage follower amplifiers as presented in Figure 8.

**Figure 8: Design for the reduction of the field effect exerted by the bulk on the sensor active area using voltage follower amplifiers.**

**Magnetic measurements**

The sensor sensitivity and linearity have been measured with a computer-controlled electromagnet by means of a spinning current method. At each field value, a current is sent between two non-adjacent contacts and the Hall voltages are recorded from the other two contacts. The voltage corresponding to the magnetic field is the mean of the Hall voltages resulting from the four contact (bias+, bias-, signal+ signal-) permutation. These phase-permutations are performed by a relay multiplexer. The residual offset was measured in a zero-Gauss chamber.

The TMAH released sensor exhibits a current and voltage related sensitivity of 1000 V/AT resp. 0.05 V/VT, a residual offset of about 0.5 mT and a non-linearity of 0.06%cso.

Figure 9 shows the measured output voltages of the four spinning phases and the resulting mean signal as a function of the applied magnetic field.

**Figure 9: Output voltage vs. magnetic field of a TMAH released VHS.**

**CONCLUSION**

A new technology providing a precise bottom release of trench MEMS structures has been presented and successfully applied to vertical Hall sensors. Moreover, a mask-less etching step to remove the polysilicon filling the trenches, which reduces the stress on the active area, has been demonstrated on SOI sensors. The tested devices showed a very high current and voltage related sensitivity and a good residual offset. However, the expected electrical linearity increase is limited by a field effect stemming from the bulk. As expected, the polysilicon etch can diminish this effect.

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**REFERENCES**


