**Current-Mode R-2R DAC**

Some deep submicron processes do not have poly-poly caps $\rightarrow$ R-2R DACs are more area efficient than charge scaling DACs.

It is possible to shift $V_{out}$ to desired range and to amplify it for the desired rail to rail swing at the cost of more power consumption.

**Voltage-Mode R-2R DAC**

$T = 1/$Sampling freq.

1-bit ADC is a simple comparator.

Finite CMRR of OpAmp can limit linearity and resolution of the DAC. Why?
**Wide Swing Current-Mode R-2R DAC**

A combination of linear thermometer code and exponential binary scaled DACs to utilize best of both.

**Segmentation in Wide Swing R-2R DAC**
Trimming DAC Offset

Offset of the OpAmp can directly affect the DAC transfer curve.

By injecting additional current into the OpAmp negative terminal it is possible to trim the offset.
**Trimming DAC Gain**

(a) DAC transfer curves before calibration. (b) DAC transfer curves after offset calibration.

5 bit MSB calibration at 32 points → Store in 32 registers for INL.

Use segmentation on the 5 MSB for DNL.

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**Trimming DAC Output**

Digital input (12) 12
Upper five bits

5-bit Register
5-bit Register
5-bit Register
5-bit Register
5-bit Register

Address 31 30 MUX
0

5

00010

00000 (upper five bits all zeroes)

R-2R ladder Fig. 30.3

R-2R circuit Fig. 30.8

R-2R ladder Fig. 30.3

Variable current

Variable voltage

R-2R ladder Fig. 30.3
R-2R DAC without OpAmp

Example: R = 10k, C_L = 10 pF
What is the fastest clock for this DAC for 10 bit accuracy?

Current Steering DAC

Using two load resistors result in generating complementary outputs for fully differential topologies.
Current Steering DAC

Series and parallel MOSFETs add up similar to resistors → We can have W-2W current mirrors that operate like R-2R ladders.

Op-Amps Used in Data Converters

The OpAmps should be designed preferably with $90^\circ$ phase margin to show a simple RC settling response and prevent any ringing.
**OpAmp Offset Trimming**

Adjust the voltage here to trim offset voltage.

**Continuous Offset Removal**

Balancing currents in the OpAmp input diff pair.
Implementing Sample and Hold

If $C = 0$ (open circuit), this topology reduces to the basic S/H in Ch. 25. See Baker P838-842.

Differential S/H

Diff in / Diff out:

Single-ended in / Diff out:
**Single-Ended to Differential S/H**

- Single-ended input
- $V_{in+} = V_{in} + V_{CM}$
- $V_{in-} = V_{CM}$

Two switches shorted together (only)

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**Fully Diff OpAmp with CMFB for S/H**

- CMFB amp detail shown in (c)

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