Logic Design

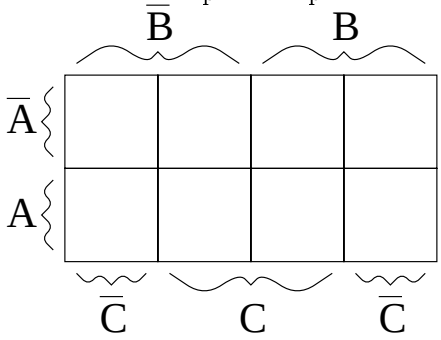
The logical function $Out = \overline{A + B\overline{C}}$ is used for each part of this function. It has the following truth table:

A	B	C	Out
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	1
1	0	1	0
0	1	1	1
1	1	1	0

Part A Implement the function using PFETs and NFETS. Your design should contain no shorts or floats.

Part B Implement the function using 2-input NOR gates and inverters. Use a MIXED LOGIC design methodology. All bubbles must be paired; all bars must be bubbled.

Part C Using the truth table above, complete the Karnaugh map below and identify the prime implicants. Then write the simplified expression. Be sure the factor out any common terms in your solution.



prime implicant	essential?
_____	yes☐ no☐
_____	yes☐ no☐
_____	yes☐ no☐

$Out =$ _____

Part D Now reimplement the simplified expression from part C using 2-input NOR gates and inverters. Use the MIXED LOGIC design methodology. All bubbles must be paired; all bars must be bubbled.