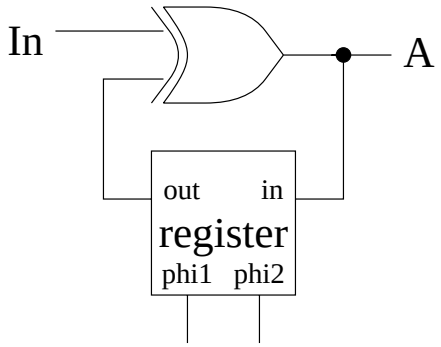
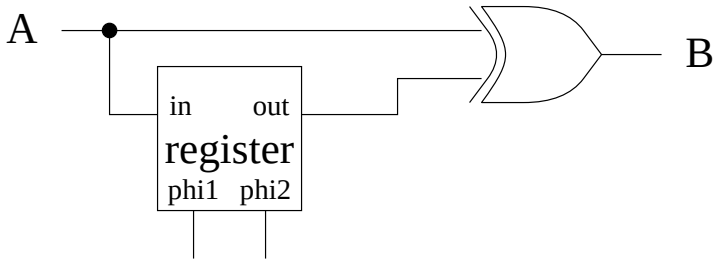
Encryption State Machine

Part A A simple encryption state machine is shown below. Compute the output pattern based on the specified input pattern (A). Assume the register initially contains a zero.



clock	1	2	3	4	5	6	7	8	9	10	11	12
In	0	1	0	1	1	0	0	1	1	1	0	1
A												
B												

Part B Now use the output from this state machine (A) as the input to another sequential logic block. Compute the output pattern assuming this register initially contains a zero (B).



Part C Now complete the problem again assuming that the registers in both circuits initially contain a one.

clock	1	2	3	4	5	6	7	8	9	10	11	12
In	0	1	0	1	1	0	0	1	1	1	0	1
A												
B												