Mixed Logic Design

Design a gate-level implementation for the following expression using the specified gate types. Use a mixed logic design methodology. All gates must either have all inputs bubbled or no inputs bubbled. Be sure that all bubbles are paired. Do *not* assume that the compliment of inputs are available. Do not simplify the expressions. Also determine the number of transistors used by your design.

Part A Implement the following expression using 2-input NOR and NOT gates.

$$F_{(A,B,C,D,E)} = \overline{A(\overline{B+C}) + \overline{D\,\overline{E}}}$$

Part B Implement the following expression using 2-input NAND and NOT gates.

$$F_{(A,B,C,D,E)} = \overline{A(\overline{B+C}) + \overline{D\,\overline{E}}}$$

Part C Implement the following expression using 2-input NOR and NOT gates.

$$F_{(A,B,C,D,E)} = \overline{\overline{\overline{A}+B+C}+D+E}$$

Part D Implement the following expression using NAND gates and inverters.

$$F_{(A,B,C,D,E)} = \overline{A\overline{B} + \overline{C\,D} + \overline{\overline{E}}}$$

Part E Implement the following expression using 2-input NAND gates and inverters.

$$F_{(A,B,C,D,E)} = \overline{A}(B + \overline{C}(\overline{D} + E))$$

Part F Implement the following expression using 2-input NAND gates and inverters.

$$Out = \overline{A}(\overline{BC} + \overline{D(E + \overline{F})})$$

Part G Implement the following expression using 2-input NOR gates and inverters.

$$Out = \overline{A}(\overline{BC} + \overline{D(E + \overline{F})})$$

Part H Implement the following expression using 2-input NOR gates and inverters.

$$F_{(A,B,C,D,E)} = \overline{\overline{(A\,\overline{\overline{B}} + C)}} + \overline{D\,E}$$

Part I Implement the following expression using 2-input NOR gates and inverters.

$$F_{(A,B,C,D,E,F)} = \overline{(A + \overline{B + C})} + \overline{D\,\overline{E}\,\overline{\overline{F}}}$$