Instruction Format Problems

1. Suppose the an instruction set architecture has an immediate instruction format with the following fields and sizes:

Opcode: 8 bits	Dest. Reg: 6 bits	Source 1 register: 6 bits	Immediate value: 20 bits

What is the maximum number of opcodes?

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What is the number of registers?

_____

What is the range of the signed immediate value?

_____

What is the instruction word size?

_____

2. Suppose a datapath has three operand busses (two source, one destination), 128 instruction types, and 64 registers where each register is 32 bits wide. Immediate operands can be in the range of ±64K. Determine the following values for the resulting instruction format. For the last two questions, assume the same operand number and types used in the MIPS format.

bits needed to specify an opcode

_____

bits needed to specify a register operand

_____

bits needed to specify an immediate operand

_____

minimum bits needed to specify an R-format instruction

_____

minimum bits needed to specify an I-format instruction

_____

3. Suppose a datapath has three operand busses (two source, one destination), 45 instruction types, and 32 registers where each register is 16 bits wide. Immediate operands can be in the range of ±128K.

Design an instruction format for instructions that have one operation, one destination register and two source registers. Label the fields and minimum number of bits need for each field.

Design an instruction format for instructions that have one operation, one destination register, one source register, and an immediate value. Label the fields and minimum number of bits need for each field.

4. Suppose we are designing an instruction set architecture with 32-bit instructions and 26 different opcodes. The register file contains 128 registers. One of the instruction types we would like to support specifies an opcode, a destination register, and two immediate source values. What is the minimum number of bits that are needed to specify each field?

Opcode: bits	Destination R: bits	Immediate value 1: bits	Immediate value 2: bits

5. Suppose we are designing an instruction set architecture with 28-bit instructions and 44 different opcodes. Immediate operands can be in the range of ±512. How many registers can this datapath have? Assume we would like to support an R-type and an I-type instruction format with the same operand number and types used in the MIPS format.