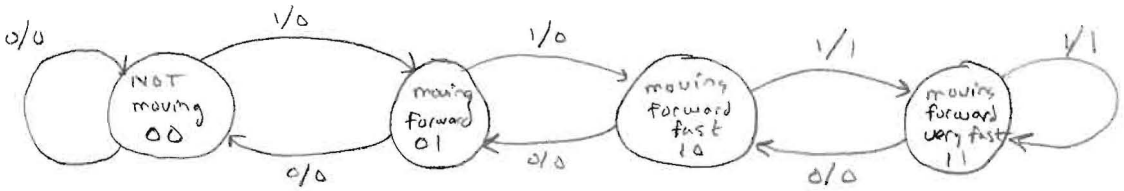
ECE2020 Test 3 Summer 2014 Georgia Tech Lorraine
July 16, 2014 Name: KEY

Calculators not allowed. **Show your work for any possible partial credit or in some cases for any credit at all** (5 pages plus a diagram page and a blank k map page, 100 possible points).

1) State Machine State Diagram:
a) (10 points) Draw the state diagram for the following speed control system for a Metz to Paris TGV train. There is one input, the train engineer has one switch which she may place in either the faster = 1 or slower = 0 position. (There is no stay at the same speed input switch position). The train has four speeds: not moving, moving forward, moving forward fast, moving forward very fast. There is one output, there is a danger light which is on when the train is in the moving very fast "state".



b) (10 points) Show the state table for the system described above.

FASTER/SLOWER	S1	S0	NS1	NS0	OUTPUT
0	0	0	0	0	0
1	0	0	0	1	0
0	0	1	0	0	0
1	0	1	1	0	0
0	1	0	0	1	0
1	1	0	1	1	1
0	1	1	1	0	0
1	1	1	1	1	1

2) State machine hardware

a) (10 points) Show the k maps and the resulting Boolean equations to implement the following state table.

input	S0	NS0	output
0	0	1	1
0	1	0	0
1	0	0	1
1	1	1	1

NS0:

INPUT \ $\overline{S0}$	$\overline{S0}$	S0
$\overline{INPUT}$	1	0
INPUT	0	1

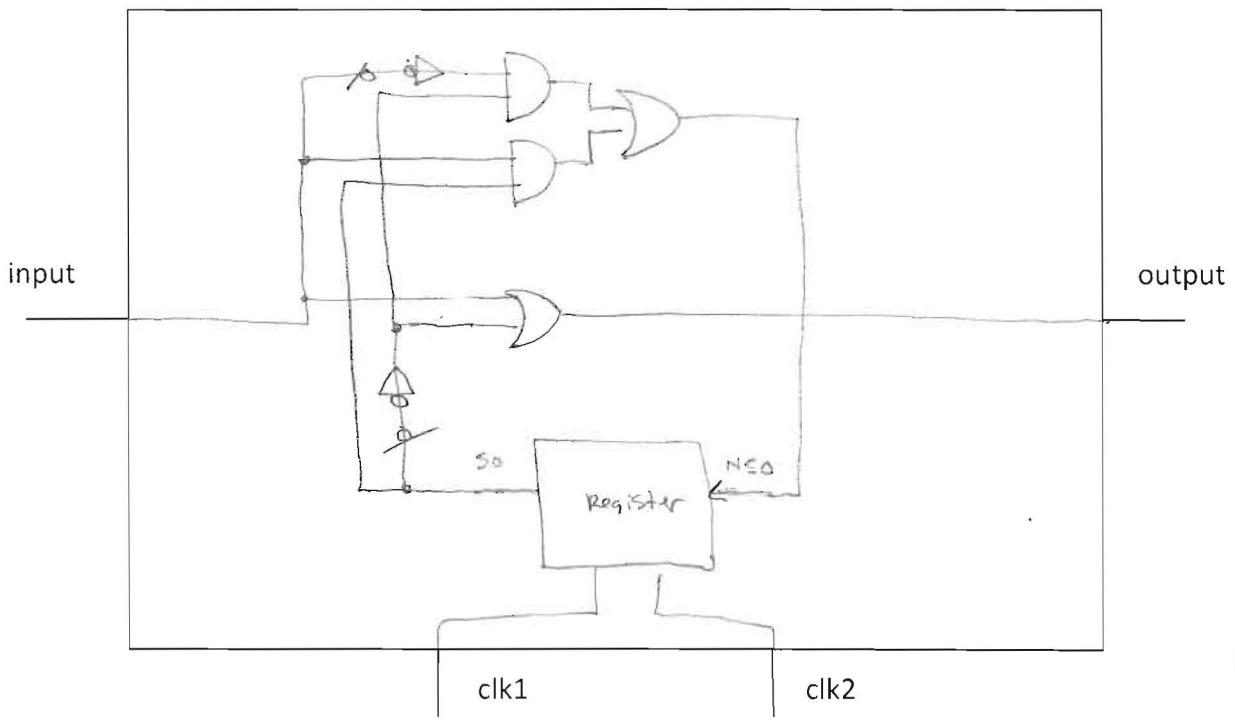
OUTPUT

INPUT \ $\overline{S0}$	$\overline{S0}$	S0
$\overline{INPUT}$	1	0
INPUT	1	1

$NS0 = \overline{INPUT} \cdot \overline{S0} + INPUT \cdot S0$

$OUTPUT = \overline{S0} + INPUT$

b) (10 points) Show all the hardware needed in the box below to implement this state machine. Be sure to include any registers you need.



3) (15 points) SIMM Memory Systems
Using SIMMs that are 1 G**Bytes** (one billion addresses by eight bit words):
Part A Suppose that these SIMMS are used to build a 4 billion address memory system with 32 bit words. Answer the following questions about this memory system:
How many address lines does each SIMM require? $2^{30} \Rightarrow 30$

How many address lines does the entire memory system require? $4 \times 2^{30} = 2^2 2^{30} = 2^{32} \Rightarrow 32$

How many SIMMS are require for the entire memory system? $\frac{32}{8}$ for each word $\times$ 4 TIMES 1 G-BYTE SIMM $= 16$ SIMMS

What kind of address decoder is required? 2 TO 4

How many memory banks are needed? 4 BANKS

4) (15 points) Suppose the following inputs (in hexadecimal) are applied to the 32-bit shift unit used in the single cycle data path shown in the diagram on the last page of the exam. Determine the output of the shift unit (in hexadecimal). You may assume the "su en" is a one to allow the shift unit to output a result.

Shift Type (st)	Input Value	Shift Amount (count)	Output
rotate	0x9B4CEF10	0x00000016	0X33BC426D
arithmetic	0x97D3AB2F	0x00010000	0XFFFF FFFF
logical	0xFFFFFFFF	0xFFFFFFFF	0XFFFFFFFE

Show your work here:

ROTATE: 0X16 => 1 0110 = 2 2 + 4 + 16 = 22 BIT POSITIONS ROTATED TO RIGHT

0X 9 B 4 C E F 1 0

1001 1011 0100 1100 1110 1111 0001 0000

BECOMES → 00 1100 1110 1111 0001 0000 1001 1011 01

3 3 B C 4 2 6 D

ARITHMETIC: SHIFT Right 0X10000 places => 1 0000 0000 0000 0000

Right 2^{16} places A HUGE AMOUNT!

SINCE MOST SIGNIFICANT IS A 1

SHIFTING RIGHT MORE THAN 32 TIMES RESULTS IN ALL ONES

RESULT 0X FFFF FFFF

LOGICAL: SHIFT AMOUNT IS NEGATIVE

negative 0X 0000 0000

+1

0X0000 0001

negative 1 SHIFT LEFT ONE BIT POSITION

RESULTS IN 0X FFFF FFFE

5) Using the datapath we have been discussing in class and shown on the last page of the exam (you may tear off that last page) write the microcode fragments to accomplish the following procedures. Use an "X" when a value is a don't care. You may assume register 0 contains all zeros. For full credit complete the description field. **Less registers used and less steps in your answers earn more credit.** Add more step #s if you need more than is drawn below.

a) (10 points) Write a microcode fragment (1 or more microinstructions) that puts the numerical value of the lower 16 bits of register 5 into register 7.

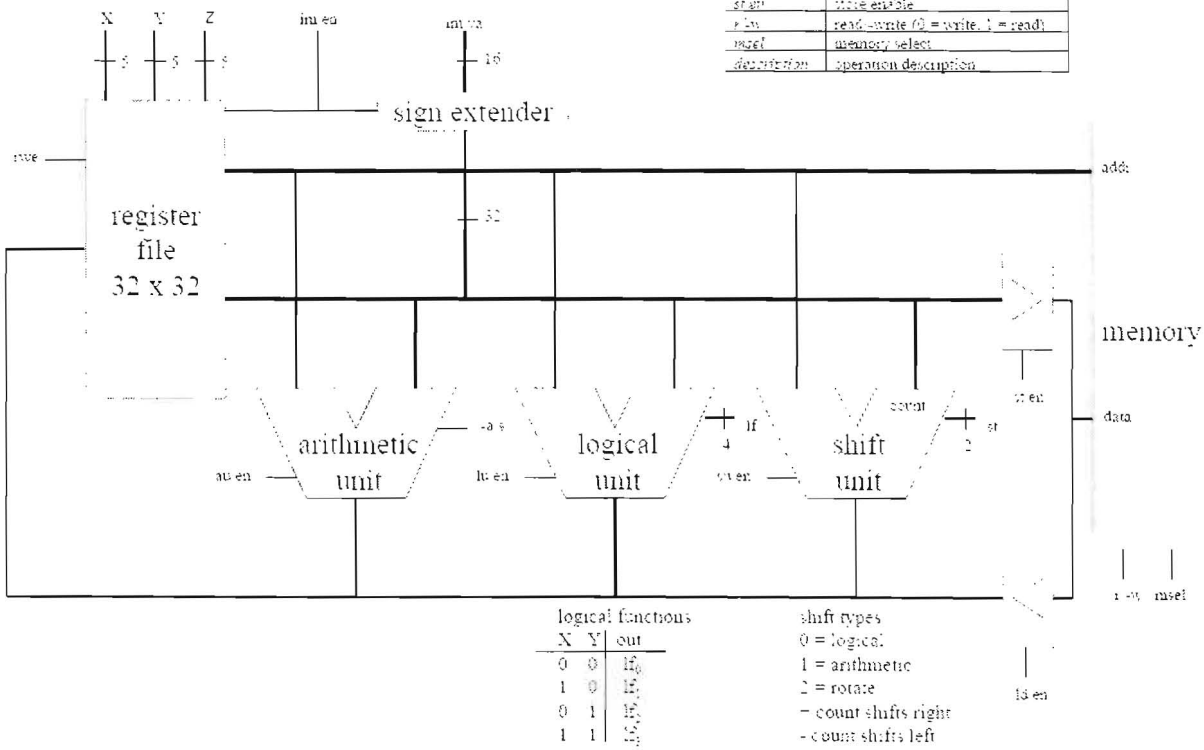
#	X	Y	Z	rwe	im en	im va	au en	-a/s	lu en	lf	su en	st	st en	ld en	r/ -w	msel	description
1	5	X	7	1	1	0X0000FFFF	0	X	1	1000	0	XX	0	0	X	0	R7 = R5 AND 0X0000FFFF
2																	
3																	
4																	
5																	

b) (20 points) Write a microcode fragment (1 or more microinstructions) that Exclusive ORs memory location 5,233 with memory location 5,500 and puts the result in memory location 6,500

#	X	Y	Z	rwe	im en	im va	au en	-a/s	lu en	lf	su en	st	st en	ld en	r/ -w	msel	description
1	X	X	1	1	1	5233	1	0	0	XXXX	0	XX	0	0	X	0	R1 = 5233
2	X	X	1	1	0	X	0	X	0	XXXX	0	XX	0	1	1	1	R1 = M[5233]
3	X	X	2	1	1	5500	1	0	0	XXXX	0	XX	0	0	X	0	R2 = 5500
4	X	X	2	1	0	X	0	X	0	XXXX	0	XX	0	1	1	1	R2 = M[5500]
5	1	2	1	1	0	X	0	X	1	alu	0	XX	0	0	X	0	R1 = R1 EXOR R2
6	X	X	2	1	1	6500	1	0	0	XXXX	0	XX	0	0	X	0	R2 = 6500
7	1	2	X	0	0	X	0	X	0	XXXX	0	XX	1	0	0	1	M[R2] = R1
8																	
9																	

cycle	cycle number
X	register driven onto X bus
Y	register driven onto Y bus
Z	register written from Z bus
rwe	register write enable
im en	immediate enable on Y bus
im val	immediate value

au en	arithmetic unit enable
au s	*subs* : sub (0 = add, 1 = subtract)
lu en	logical unit enable
lf	logical function
su en	shift unit enable
st	shift type
ld en	load enable
st en	store enable
r/w	read-write (0 = write, 1 = read)
msel	memory select
description	operation description



logical functions

X	Y	out
0	0	lf_0
1	0	lf_1
0	1	lf_2
1	1	lf_3

shift types
0 = logical
1 = arithmetic
2 = rotate
– count shifts right
- count shifts left

K MAPS: