ECE2020 Test 2 Summer 2014 GTL Name: _____
June 27, 2014
Calculators not allowed. **Show your work for any possible partial credit or in some cases for any credit at all.** Note the last page shows you some blank K maps just in case you need them on this exam. 6 pages, possible 100 points.

Problem 1 (20 points) For the bit representations below, determine the most negative value, most positive value, and step size (difference between sequential values). All answers must be expressed in decimal notation just like the practice problems we did in class (using k, M notation). Fractions (for example 3/16ths) must be used. All signed representations are two's complement signed numbers. You must show your work.

representation	most negative value	most positive value	step size
unsigned integer (15 bits). (0 bits)			
Signed integer (15 bits). (0 bits)			
unsigned fixed-point (15 bits). (8 bits)			
signed fixed-point (15 bits). (8 bits)			

Problem 2 Part A Arithmetic (10 points) For each problem below, compute the operations using the rules of arithmetic, and indicate whether an overflow occurs assuming all numbers are expressed using a five bit **unsigned** representation

0 1 0 1 1	0 1 1 0 1
+ 1 1 0 0 1	+ 0 0 1 0 0

result

_____

unsigned
error?

_____

Problem 2 Part B Arithmetic (10 points) For each problem below, compute the operations using the rules of arithmetic, and indicate whether an overflow occurs assuming all numbers are expressed using a a five bit **signed** two's complement representations.

0 1 0 1 1	1 0 1 1 1	0 1 0 0 0	1 0 0 1 1
+ 0 1 1 0 1	+ 0 1 0 0 1	- 0 0 1 0 1	- 0 0 1 1 0

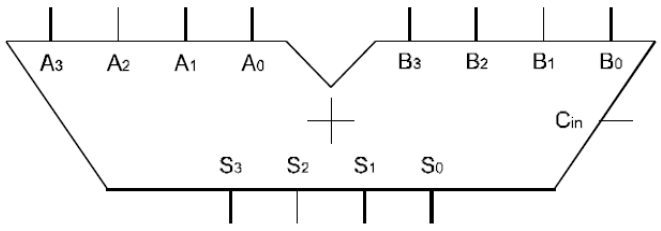
result

_____

signed
error?

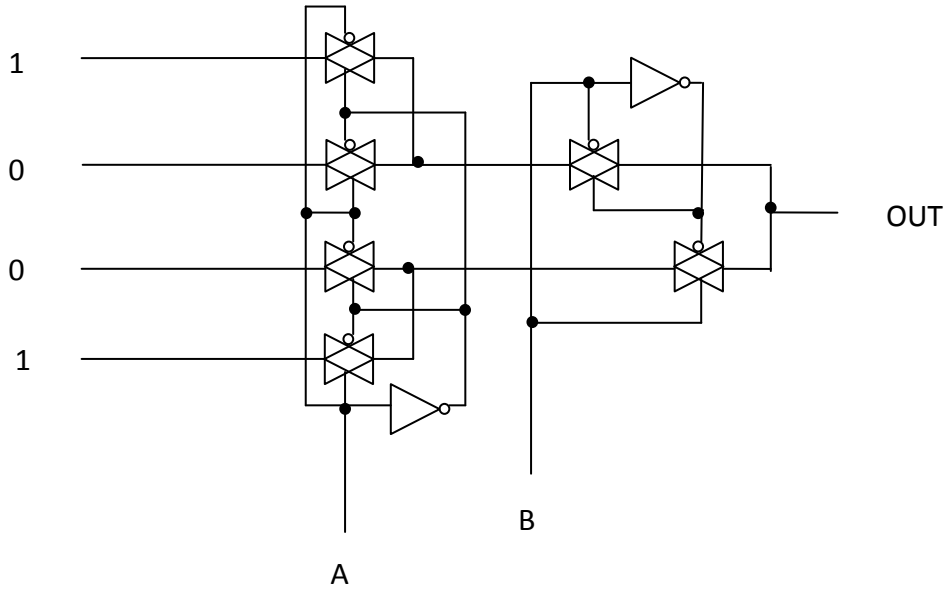
_____

Problem 2 part C Arithmetic (10 points) The adder below adds two four bit numbers X and Y and produces a four bit result S. Add the digital logic to support subtraction as well as addition. Label inputs X_3, X_2, X_1, X_0, Y_3, Y_2, Y_1, Y_0, as well as outputs Z_3, Z_2, Z_1, Z_0. Do not put in the circuitry to determine errors.



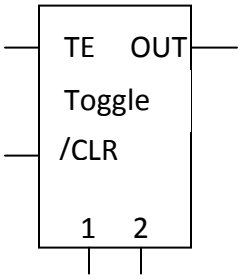
3) (10 points) Complete the truth table for the following logic block.

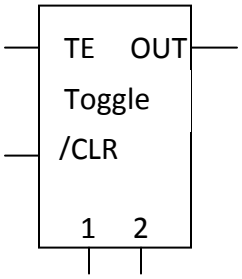
A	B	OUT
0	0	
0	1	
1	0	
1	1	

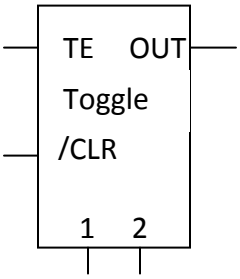


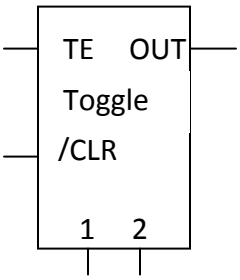
What boolen function (if any) does the circuit implement? _____

4) Counters (10 points) Connect the toggle cells below to build a divide by 11 counter. Be sure to include an external Count Enable and an external active high clear. Include any circuitry needed to allow this to work in multiple digit counters (like in an alarm clock). You do not have to used mixed logic.

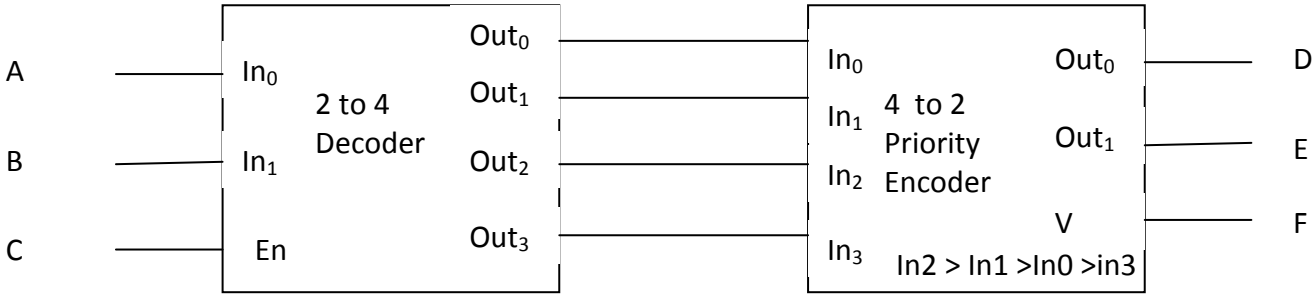






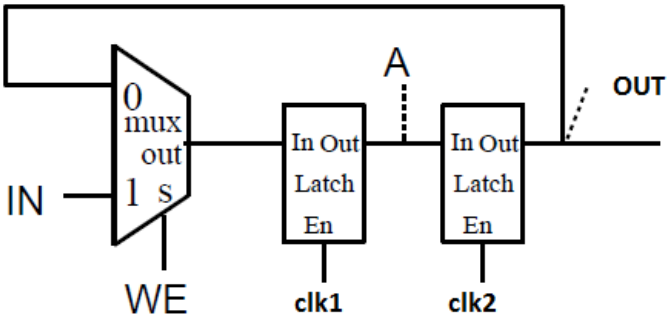


5) (15 points) Consider the following circuit. For each combination of inputs listed below, determine the corresponding outputs. You must show your work and reasoning for any credit. Do not just put an answer without explaining.



A	B	C	D	E	F
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

6) Registers (15 points) Consider the register implementation below.



Assume the following signals are applied to the register above. Draw the signal at point A (output of the first latch), the signal at point OUT (output of second latch). Assume A and OUT start at unknown values which are shown below as both a high and a low at the same time with cross hatches drawn between the two values.