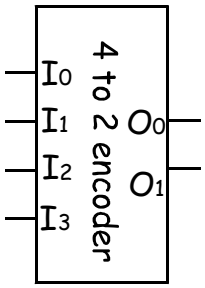
Problem 1 (4 parts, 21 points) Encoders and Pass Gates

Part A (8 points) Suppose the circuit below has the following input priority: $I_1 > I_3 > I_0 > I_2$. Complete the truth table by filling in the input values that would produce the given outputs and derive a simplified expression for O_1.



I_3	I_2	I_1	I_0	V	O_1	O_0
0	0	0	0	0	X	X
0	X	0	1	1	0	0
X	X	1	X	1	0	1
0	1	0	0	1	1	0
1	X	0	X	1	1	1

$O_1 =$ $\overline{I}_1(\overline{I}_0 + I_3)$

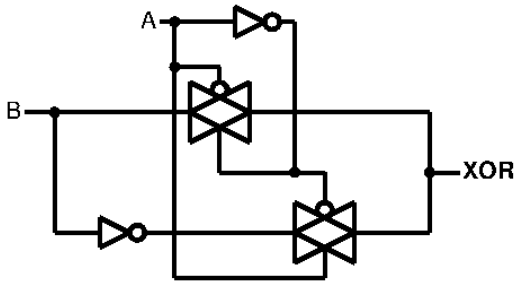
Part B (3 points) Consider a priority encoder with the following behavior:

In_2	In_1	In_0	Valid	Out_1	Out_0
0	0	0	0	x	x
0	0	1	1	0	0
0	1	0	1	0	1
0	1	1	1	0	1
1	0	0	1	1	0
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	1	0	1

List the inputs (In_0, In_1, and In_2) in decreasing priority.

In_1 (highest priority) > **In_0** (2nd highest priority) > **In_2** (lowest priority)

Part C (6 points) Implement a 2-input XOR gate with pass gates and inverters only. (Hint: remember that a 2-input XOR is a selective inverter.)



Part D (4 points) Does your implementation of an XOR in Part C require fewer transistors than the gate's standard switch-level implementation? Circle one: **Yes**

Support your answer by giving the transistor count for each:

 # transistors in Part C implementation: 8 **# transistors in switch-level XOR implementation: 12**

Problem 2 (3 parts, 24 points) Number Systems

Part A (10 points) Convert the following notations:

binary notation	decimal notation
0101 1101.1	**93.5**
110100.01	52.25
110 0110.101	**102.625**
hexadecimal notation	**octal notation**
0x12B.54	453.25
0xB357.6C	**131527.33**

Part B (8 points) For the 26 bit representations below, determine the most positive value and the step size (difference between sequential values). **Express all answers in decimal notation**. Fractions (e.g., 3/16ths) may be used. Signed representations are two's complement.

representation	most positive value	step size
unsigned integer (26 bits) . (0 bits)	**2^{26} = 64M**	**1**
signed fixed-point (19 bits) . (7 bits)	**2^{18} = 256K**	**1/128**
signed integer (26 bits) . (0 bits)	**2^{25} = 32M**	**1**
signed fixed-point (23 bits) . (3 bits)	**2^{22} = 4M**	**1/8**

Part C (6 points) A 20 bit floating point representation has a 12 bit mantissa field, a 7 bit exponent field, and one sign bit.

What is the largest value that can be represented (closest to infinity)? 2^{63}

What is the smallest value that can be represented (closest to zero)? 2^{-64}

How many decimal significant figures are supported? **3**

Problem 3 (3 parts, 30 points) Computation

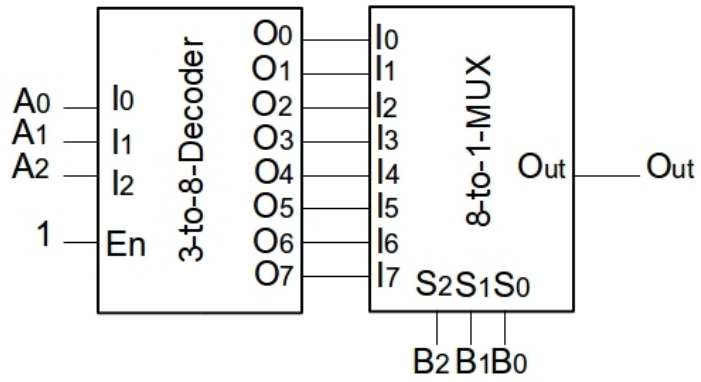
Part A (12 points) For each problem below, compute the operations using the rules of arithmetic, and indicate whether an overflow occurs assuming all numbers are expressed using a **six bit unsigned** and **six bit two's complement** representations.

	100101 + 101011	10101 + 101100	110111 - 011001	11100 - 10100
result	**010000**	**000001**	**011110**	**01000**
unsigned error?	**Yes**	**Yes**	**No**	**No**
signed error?	**Yes**	**No**	**Yes**	**No**

Part B (8 points) For each bit string below, what is the decimal number it represents if it uses a 5-bit unsigned representation and if it uses a 5-bit two's complement representation?

Bit string	Decimal (if unsigned representation)	Decimal (if 2's complement signed representation)
01101	**13**	**+13**
11110	**30**	**-2**
1111.1	**15.5**	**-0.5**
011.11	**3.75**	**+3.75**

Part C (10 points) Consider the circuit below. Complete the truth table by filling in the empty boxes. (Note that there may be multiple possible inputs that can result in a given output; you need to show only one.) Finally, state what condition this circuit tests on the two input words **A** and **B** (which are each 3-bit words: $A_2A_1A_0$ and $B_2B_1B_0$).



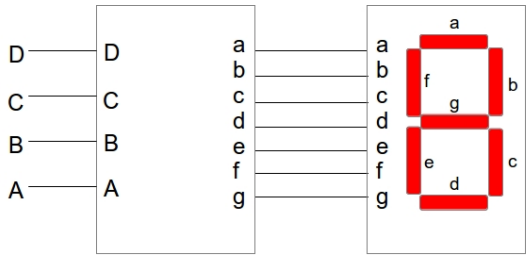
A_2	A_1	A_0	B_2	B_1	B_0	Out
1	1	0	1	1	0	**1**
0	1	0	**0**	**1**	**0**	1
1	0	1	0	1	0	**0**
1	0	0	**1**	**1**	**1**	0

(any B except 100)

This circuit's **Out** signal is high if **A** **equals** **B.**

Problem 4 (4 parts, 25 points) Decoding

Suppose you are implementing a seven segment display as shown below. Input decimal numbers are represented as unsigned binary numbers DCBA (e.g., 0101 = 5, which is displayed by lighting segments **a**, **c**, **d**, **f**, and **g**). *In this problem, unlike the Homework 2 problem, assume that for input decimal numbers greater than 9, the 7-segment display is blank (no segments are lit up).*



Part A (4 points) Complete the BCD to 7-segment decoder truth table below by filling in the Decoder Output column for **a**.

Binary Inputs				Decoder Outputs							7-Segment Display Outputs
D	**C**	**B**	**A**	**a**	**b**	**c**	**d**	**e**	**f**	**g**	
0	0	0	0	**1**	1	1	1	1	1	0	0
0	0	0	1	**0**	1	1	0	0	0	0	1
0	0	1	0	**1**	1	0	1	1	0	1	2
0	0	1	1	**1**	1	1	1	0	0	1	3
0	1	0	0	**0**	1	1	0	0	1	1	4
0	1	0	1	**1**	0	1	1	0	1	1	5
0	1	1	0	**1**	0	1	1	1	1	1	6
0	1	1	1	**1**	1	1	0	0	0	0	7
1	0	0	0	**1**	1	1	1	1	1	1	8
1	0	0	1	**1**	1	1	1	0	1	1	9
1	0	1	x	0	0	0	0	0	0	0	no segments turned on
1	1	x	x	0	0	0	0	0	0	0	no segments turned on

Part B (6 points) Write the standard sum of products form of Decoder Output **e**.

e = $\overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\overline{D}+\overline{A}\cdot B\cdot\overline{C}\cdot\overline{D}+\overline{A}\cdot B\cdot C\cdot\overline{D}+\overline{A}\cdot\overline{B}\cdot\overline{C}\cdot D$

Part C (6 points) For which decimal numbers is the following expression true? Assume each decimal number is represented as an unsigned binary number DCBA.

$$W=\overline{D}+\overline{B}\cdot\overline{C}$$

Decimal numbers: **0, 1, 2, …, 9**

Part D (9 points) Implement Decoder Output **e** using a single 4-to-16 decoder (with an enable) and a single OR gate. The OR gate may have any number of inputs that you need. Label all input and output signals on the decoder. Assume you are given the inputs A, B, C, D, and the input $W = \overline{D} + \overline{B} \cdot \overline{C}$ (which is provided by another circuit that you do not need to implement).