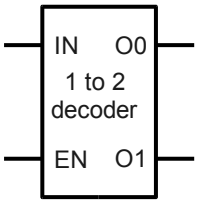
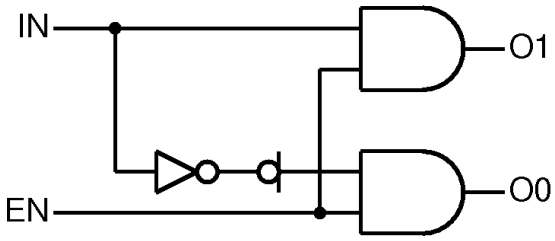
Problem 1 (3 parts, 24 points) Decoding Decoders

Part A (6 points) Define a 1 to 2 decoder by completing the behavior table.

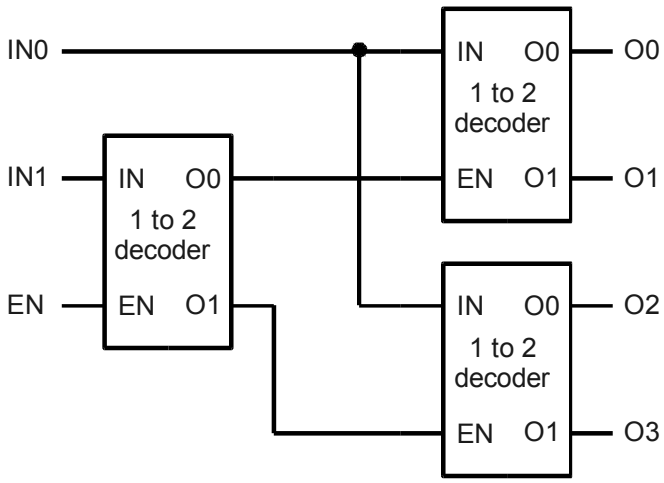
IN	EN	O0	O1
X	0	0	0
0	1	1	0
1	1	0	1



Part B (8 points) Implement a 1 to 2 decoder using basic gates. Assume only true (non-complemented) inputs are available. Label all inputs and outputs.



Part C (10 points) Using *only* the three 1 to 2 decoders shown below, implement a 2 to 4 decoder with an enable. Label the decoder inputs (IN_1, IN_0, EN) and outputs (O0, O1, O2, O3).



Problem 2 (2 parts, 18 points) "Get your priorities right!"

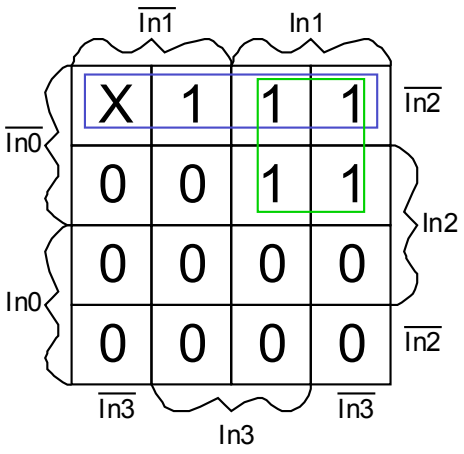
Consider a priority encoder with the following behavior:

In_3	In_2	In_1	In_0	Valid	O_1	O_0
0	0	0	0	0	X	X
X	X	X	1	1	0	0
X	X	1	0	1	0	1
X	1	0	0	1	1	0
1	0	0	0	1	1	1

Part A (8 points) List the inputs (In_0, In_1, In_2, and In_3) in increasing priority.

In_3	<	In_2	<	In_1	<	In_0
lowest priority		3rd highest priority		2nd highest priority		highest priority

Part B (10 points) Express the behavior of O_0 in the map below. Derive a simplified ***sum of products*** expression using a Karnaugh Map. Circle and list the prime implicants, indicating which are essential. Then write the simplified SOP expression.



prime implicants	essential? yes	no
$\overline{In0}\ \overline{In2}$	☒	☐
$\overline{In0}\ In1$	☒	☐
	☐	☐
	☐	☐
	☐	☐
	☐	☐
	☐	☐
	☐	☐

$O_0 = \overline{In0}\cdot(In1+\overline{In2})$

Problem 3 (4 parts, 40 points) Number Systems & Arithmetic

Part A (10 points) Convert the following notations:

binary notation	**decimal notation**
1101 1011.	219
101 1100.1101	92.8125
11011.101	27.625
binary notation	**hexadecimal notation**
1 0010 0101.1101 11	125.DC
1100 1011 0100.0010 1011 0001	CB4.2B1

Part B (12 points) For the 22 bit representations below, determine the most positive value and the step size (difference between sequential values). **All answers should be expressed in decimal notation**. Fractions (e.g., 3/16ths) may be used. Signed representations are two's complement.

representation	most positive value	step size
unsigned integer (22 bits) . (0 bits)	4M	1
signed fixed-point (18 bits) . (4 bits)	128K	1/16
signed fixed-point (14 bits) . (8 bits)	8K	1/256
signed fixed-point (11 bits) . (11 bits)	1K	1/2K

Part C (6 points) A 16 bit floating point representation has a 10 bit mantissa field, a 5 bit exponent field, and one sign bit.

What is the largest value that can be represented (closest to infinity)? 2^{15}

What is the smallest value that can be represented (closest to zero)? 2^{-16}

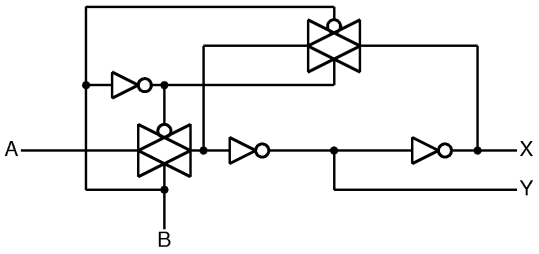
How many decimal significant figures are supported? 3

Part D (12 points) For each problem below, compute the operations using the rules of arithmetic, and indicate whether an overflow occurs assuming all numbers are expressed using a **five bit unsigned fixed-point** and **five bit two's complement fixed-point** representations.

	10.11 + 11.01	111.10 + 1.01	100.01 - 10.11	1.11 - 10.00
result	110.00	000.11	001.10	111.11
unsigned error?	■ no □ yes	□ no ■ yes	■ no □ yes	□ no ■ yes
signed error?	□ no ■ yes	■ no □ yes	□ no ■ yes	■ no □ yes

Problem 4 (3 parts, 18 points) "Does this register?"

Part A (6 points) Express the behavior of the circuit below. Use standard symbols (0, 1, X, Z_0, Q_0, etc.). Then name the circuit.

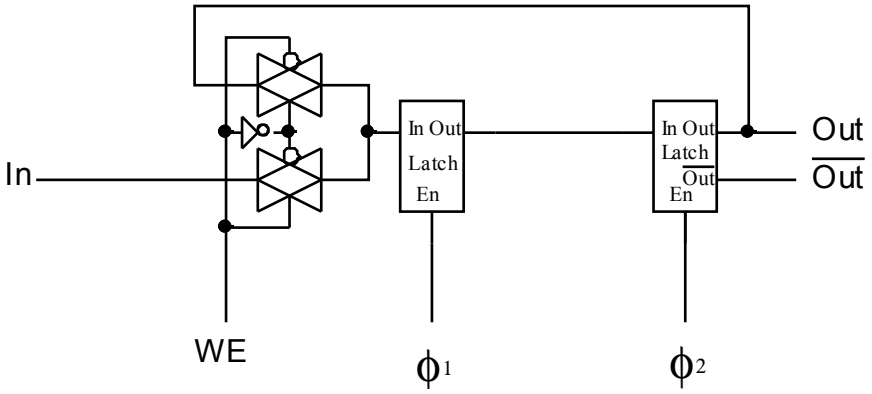


A	B	X	Y
0	0	Q_0	$\overline{Q}_0$
1	0	Q_0	$\overline{Q}_0$
0	1	0	1
1	1	1	0

This circuit is a Transparent Latch

Part B (6 points) Implement a register below using *only* latches, pass gates, and inverters (all in icon form). Complete the behavior table at right. Recall that the CLK signal indicates a full Φ_1 Φ_2 cycle; so the output should be the value at the end of a cycle (for the given inputs).

In	WE	Clk	Out	$\overline{Out}$
A	0	↑↓	Q_0	$\overline{Q}_0$
A	1	↑↓	A	$\overline{A}$



Part C (6 points) Assume the following signals are applied to your register. Draw the output signal **Out**. Draw a vertical line where **In** is sampled. *Draw crosshatch where **Out** is unknown.*