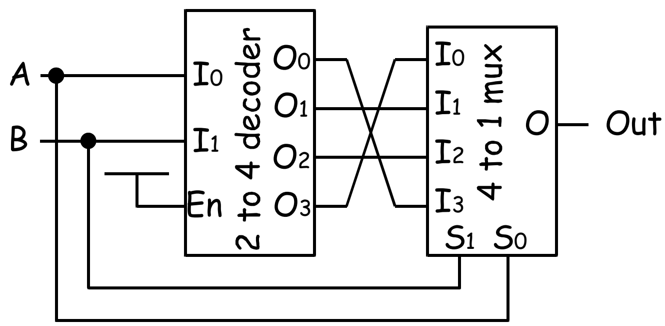
Problem 1 (3 parts, 24 points) Building Blocks

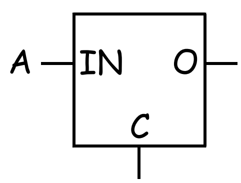
Part A (8 points) Consider the circuit below. Complete the truth table. Then state what logical function this circuit implements.



A	B	Out
0	0	0
1	0	1
0	1	1
1	1	0

This wacky circuit is a Odd Parity (XOR)

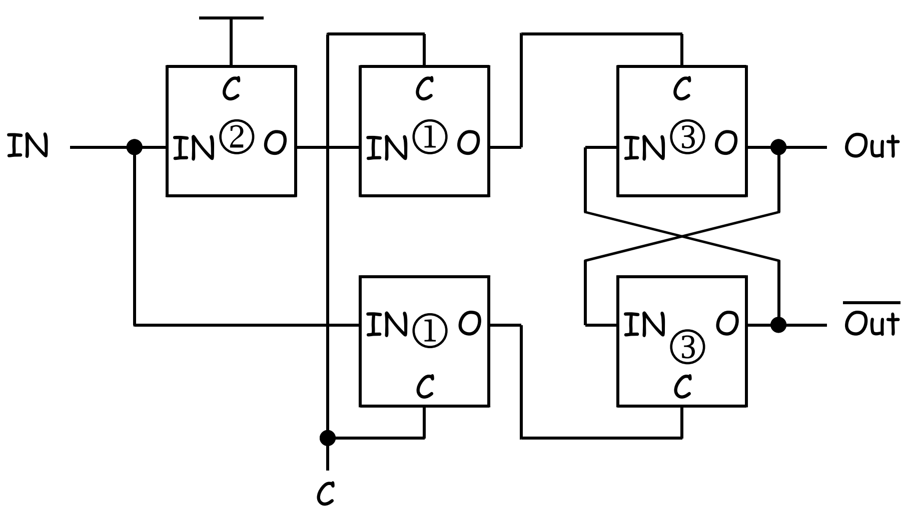
Part B (8 points) Consider four different building block definitions below. The symbolic value *A* is presented at its input. The control input and resulting out are shown in the truth table. Name the *logical gate or gates* that implement each definition.



In	C	①	②	③	④
A	0	0	A	$\overline{A}$	Z_o
A	1	A	$\overline{A}$	0	A

① AND ② XOR ③ NOR ④ Pass & NOT

Part C (8 points) Blocks from part B are used to create a new module below. The symbolic value *A* is presented at its input. Complete the truth table and give its functional name.



IN	C	Out
A	0	Q_o
A	1	A

It's a: transparent latch

Problem 2 (3 parts, 28 points) Number Systems

Part A (10 points) Convert the following notations:

binary notation	**decimal notation**
1010 1010.	128+32+8+2 = 170
0101 0101.1001	64+16+4+1+.5+.0625 = 85.5625
1111 1111.1111	255.9375
octal notation	**hexadecimal notation**
5755.7	1011 1110 1101.1110 = BED.E
33.33	0001 1011.0110 1100 = 1B.6C

Part B (12 points) For the 24 bit representations below, determine the most positive value and the step size (difference between sequential values). **All answers should be expressed in decimal notation**. Fractions (e.g., 3/16ths) may be used. Signed representations are two's complement.

representation	most positive value	step size
unsigned integer (24 bits) . (0 bits)	16M	1
signed fixed-point (18 bits) . (6 bits)	128K	1/64
signed fixed-point (15 bits) . (9 bits)	16K	1/512
signed fixed-point (12 bits) . (12 bits)	2K	1/4K

Part C (6 points) A 48 bit floating point representation has a 37 bit mantissa field, a 10 bit exponent field, and one sign bit.

What is the largest value that can be represented (closest to infinity)? 2^{511}

What is the smallest value that can be represented (closest to zero)? 2^{-512}

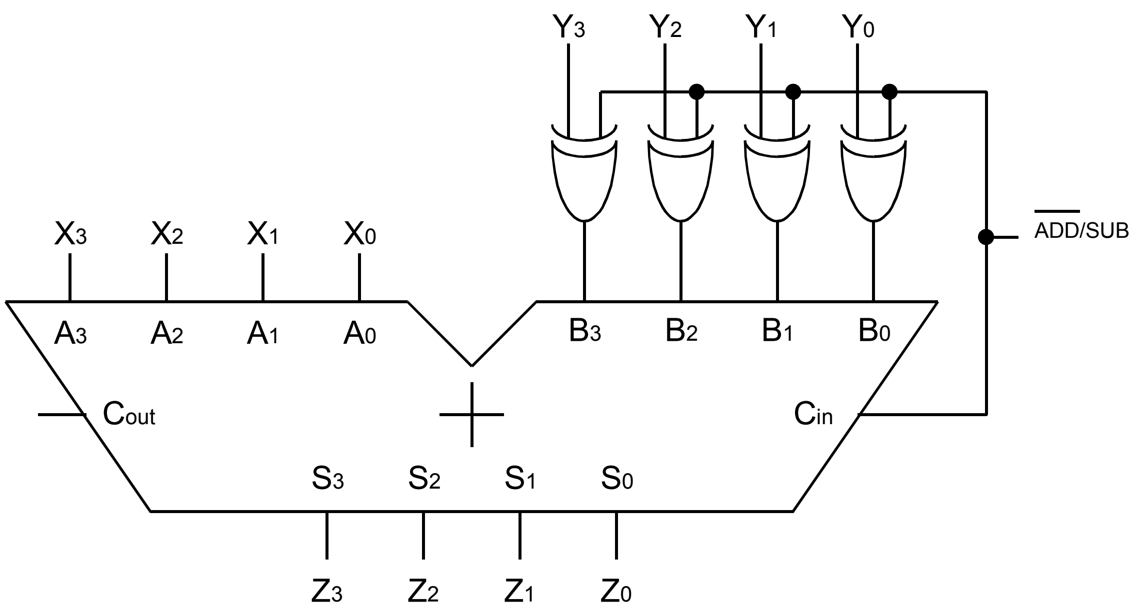
How many decimal significant figures are supported? 11

Problem 3 (3 parts, 24 points) "Math is easy"

Part A (12 points) For each problem below, compute the operations using the rules of arithmetic, and indicate whether an overflow occurs assuming all numbers are expressed using a **six bit unsigned fixed-point** and **six bit two's complement fixed-point** representations.

	111.010 + 111.011	11.111 + 0.001	100.000 - 10.001	10.101 - 101.010
result	110.101	100.000	1.111	101.011
unsigned error?	yes	no	no	yes
signed error?	no	yes	yes	yes

Part B (6 points) The adder below adds two four bit numbers A and B and produces a four bit result S. Add extra digital logic to support subtraction as well as addition. Label inputs X_3, X_2, X_1, X_0, Y_3, Y_2, Y_1, Y_0, $\overline{ADD}/SUB$ and outputs Z_3, Z_2, Z_1, Z_0.



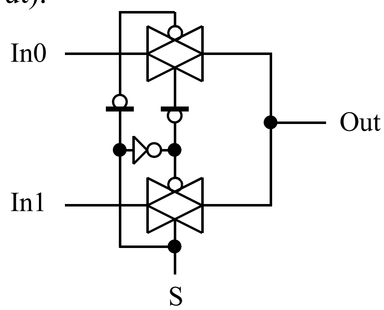
Part C (6 points) Write two Boolean expressions indicating signed two's compliment addition and subtraction overflow using inputs X_3, Y_3, Z_3. These SOP expressions should be true when overflow occurs.

addition overflow = $X_3 \cdot Y_3 \cdot \overline{Z_3} + \overline{X_3} \cdot \overline{Y_3} \cdot Z_3$

subtraction overflow = $X_3 \cdot \overline{Y_3} \cdot \overline{Z_3} + \overline{X_3} \cdot Y_3 \cdot Z_3$

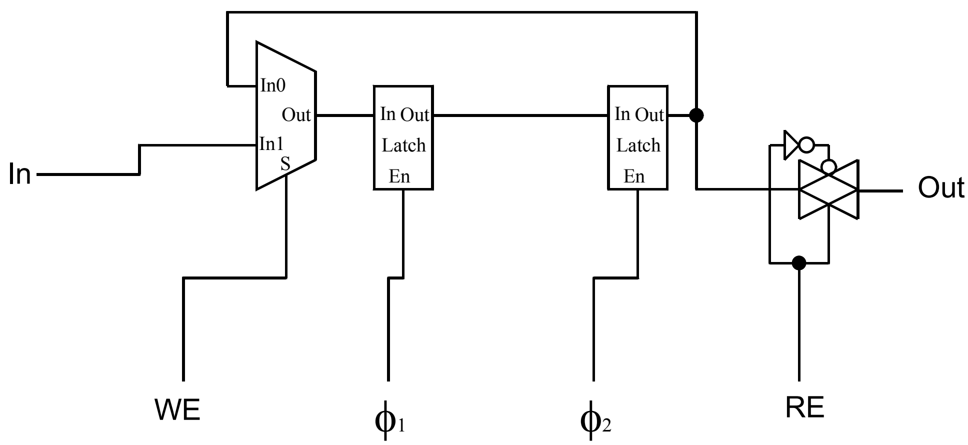
Problem 4 (3 parts, 24 points) "Register your knowledge"

Part A (8 points) Implement a 2 to 1 multiplexer using only pass gates and inverters. Label all inputs (IN_0, IN_1, S) and output (Out).



Part B (10 points) Implement a register below using needed muxes, latches, pass gates, and inverters (all in icon form). Complete the behavior table at right. Recall that the CLK signal indicates a full Φ_1 Φ_2 cycle; so the output should be the value at the end of a cycle (with the given inputs).

In	WE	RE	Clk	Out
A	0	0	↑↓	Z_o
A	1	0	↑↓	Z_o
A	0	1	↑↓	Q_o
A	1	1	↑↓	A



Part C (6 points) Assume the following signals are applied to your register. Draw the output signal **Out**. Draw a vertical line where **In** is sampled. *Draw crosshatch where **Out** is unknown.*