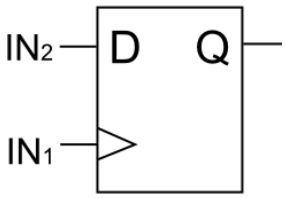
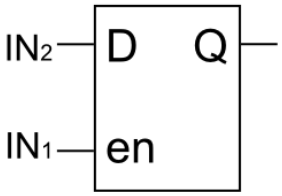
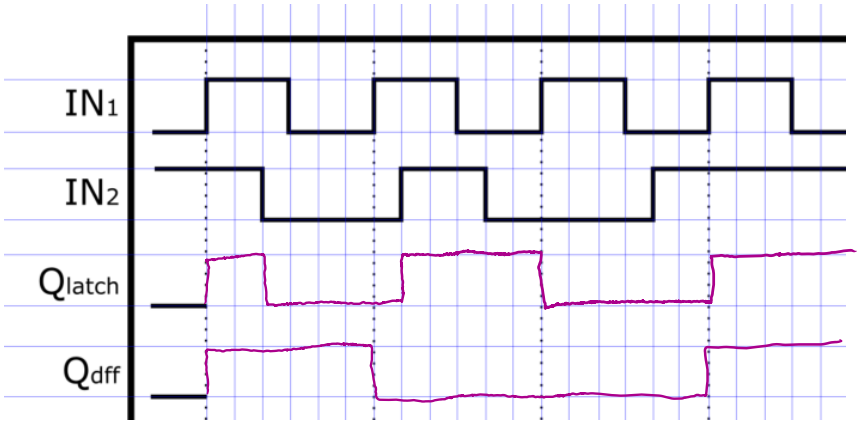
Question 1) (25 points)

Assume the following connections to signals IN1 and IN2:

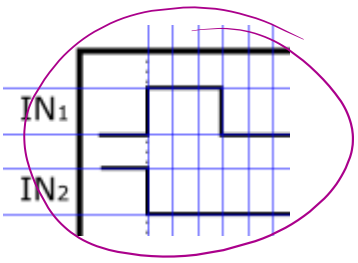


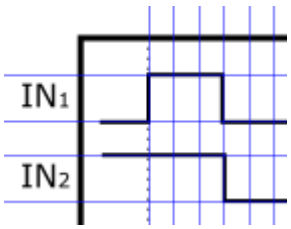


a) Perform a functional simulation for Q_{latch} and Q_{dff} (i.e. not accounting for propagation delay).

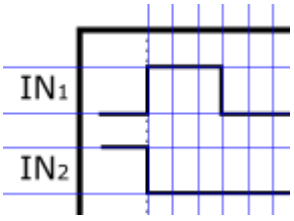


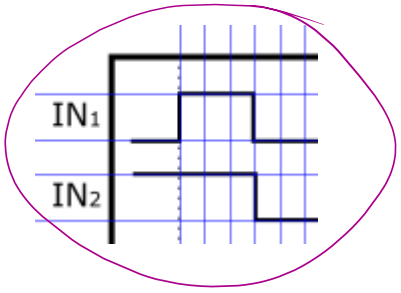
b) Which of the following violate timing requirements of a flip-flop. Circle neither, one, or both.





c) Which of the following violate timing requirements of a latch. Circle neither, one, or both.

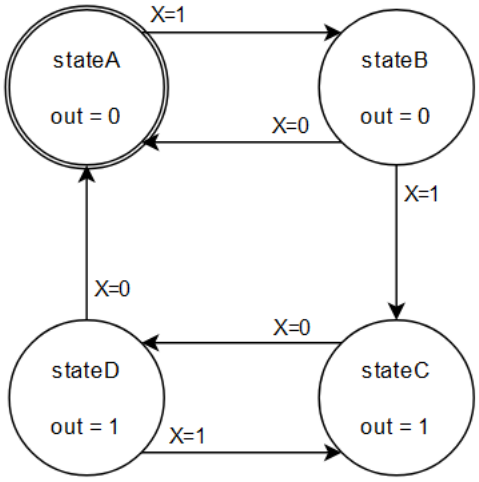




what value of D would end up being finally latched?

Question 2) (15 points)

If you were implementing this state machine in digital hardware:



a) What is the minimum number of flip-flops that you would need?

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b) Could stateC and stateD be combined into a single state without changing the behavior of the state machine?

Yes / (No) (circle one)

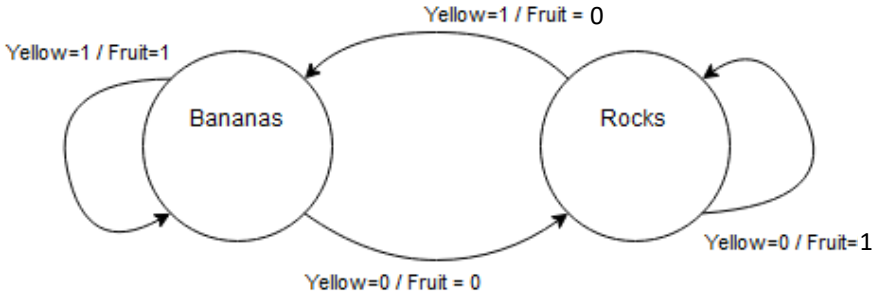
c) Does the Boolean expression for the output logic need to include the X signal (the state machine input)?

Yes / (No) (circle one)

Question 3) (10 points)

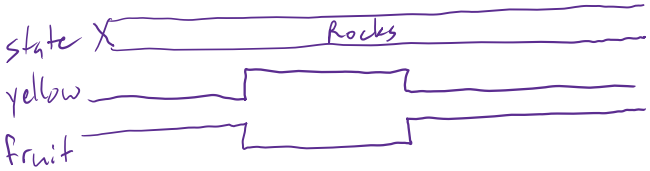
Consider this Mealy-style state diagram:

The state machine input is a signal named "Yellow", and the output is a signal named "Fruit".



Explain whether it is or is not possible to construct a Moore state machine with the same behavior, and why or why not. (This should only need one sentence; don't spend a lot of time writing a lengthy explanation.)

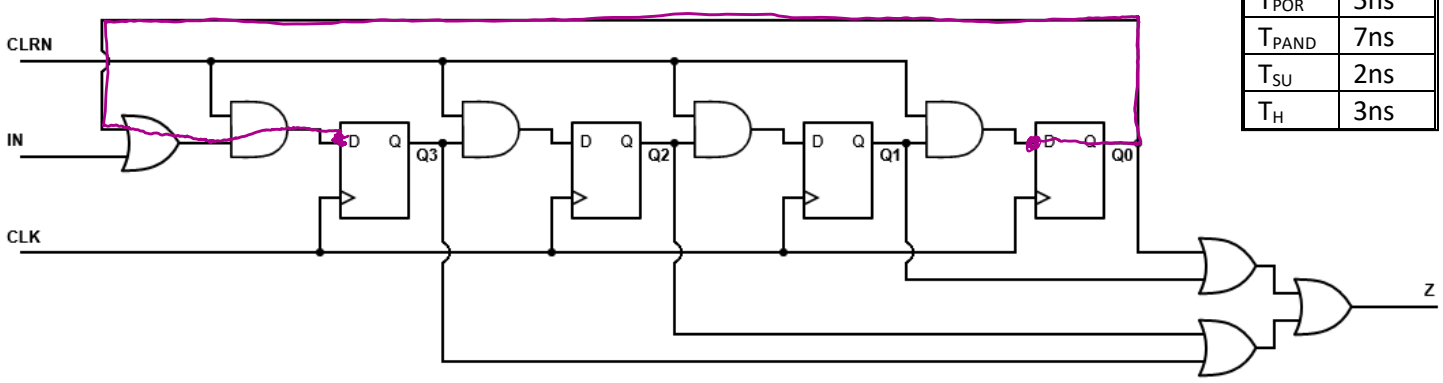
No. Simple counter example:



This is impossible to achieve with a Moore state machine.

Question 4) (30 points)

T_{PDFF}	11ns
T_{POR}	5ns
T_{PAND}	7ns
T_{SU}	2ns
T_H	3ns



a) Complete the blank entries in the following transition table based on the state machine above. The state "names" are the same as the state encodings Q_3-Q_0.

Current State	Input CLRN	Input IN	Next State	Output Z
0000	0	1	0000	0
0000	1	0	0000	0
0000	1	1	1000	0
0101	0	1	0000	1
0101	1	0	1010	1
0101	1	1	1010	1

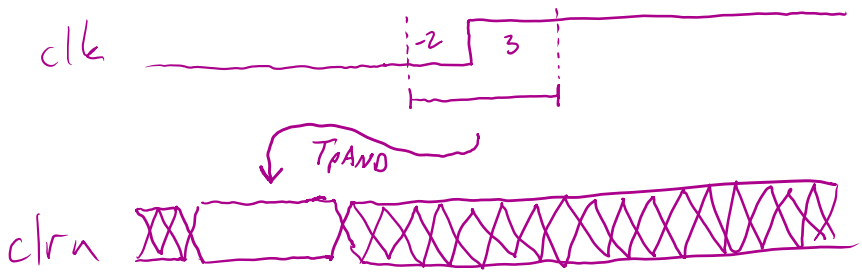
b) What is the maximum frequency at which this state machine can be safely clocked? Express your answer as a mathematical expression in terms of the parameters in the table above (i.e., do not calculate a final value).

$1/(T_{pdff} + T_{por} + T_{pAND} + T_{su})$ see relevant propagation path on diagram.

c) After a rising clock edge, how long do you have to wait before the output (Z) is guaranteed to be correct? Express your answer in terms of the given parameters (i.e. do not calculate a final value).

$T_{PDFF} + 2 \cdot T_{POR}$

d) If a rising clock edge occurs at time t=0, during what period of time should input CLRN not change? Express your answer as a range; for example -3ns to +2ns.



-9 to -4 ns

Question 5) (20 points)

Draw a state diagram for a Moore state machine that meets the following requirements. This state machine is intended for hardware implementation with digital logic, so all signals are binary signals and the state machine is clocked.

- The state machine has two inputs named Left and Up.
- The state machine has one output named Spin.
- At any time, if Left is active and Up is inactive for two consecutive clock cycles, output Spin should be asserted and should then remain active as long as Left remains active, regardless of Up. If Left goes inactive while Spin is active, Spin should be deasserted on the next clock edge.