ECE2020 A Fall 2018 Test 2

Name: _____

- Only a writing implement may be used on this exam (i.e. no books, notes, or any electronics).
- If the meaning of any question is not clear, please ask for clarification.
- Partial credit can only be awarded for work shown.

Honor pledge:

On my honor, I pledge that I will neither receive nor provide improper assistance in the completion of this test. I understand and accept my responsibility as a member of the Georgia Tech Community to uphold the Honor Code at all times, and I know that I have options for reporting honor violations at osi.gatech.edu. Thanks for reading all the way through.

GTID: _____ Signature: _____

Boolean Identities

Identity	$A + 0 = A$	$A \cdot 1 = A$
Dominance	$A + 1 = 1$	$A \cdot 0 = 0$
Idempotence	$A + A = A$	$A \cdot A = A$
Inverse	$A + \overline{A} = 1$	$A \cdot \overline{A} = 0$
Commutative	$A + B = B + A$	$A \cdot B = B \cdot A$
Associative	$A + (B + C) = (A + B) + C$	$A \cdot (B \cdot C) = (A \cdot B) \cdot C$
Distributive	$A \cdot (B + C) = A \cdot B + A \cdot C$	$A + B \cdot C = (A + B) \cdot (A + C)$
Absorption	$A \cdot (A + B) = A$	$A + A \cdot B = A$
DeMorgan's	$\overline{(A + B)} = \overline{A} \cdot \overline{B}$	$\overline{(A \cdot B)} = \overline{A} + \overline{B}$
Double Complement	$\bar{\bar{A}} = A$	
FOIL	$(A + B) \cdot (C + D) = A \cdot C + A \cdot D + B \cdot C + B \cdot D$	
Disappearing opposite	$A + \overline{A} \cdot B = A + B$	

Decimal	Binary	Hex
0	0	0
1	1	1
2	10	2
3	11	3
4	100	4
5	101	5
6	110	6
7	111	7
8	1000	8
9	1001	9
10	1010	A
11	1011	B
12	1100	C
13	1101	D
14	1110	E
15	1111	F

2^{-6}	0.015625
2^{-5}	0.03125
2^{-4}	0.0625
2^{-3}	0.125
2^{-2}	0.25
2^{-1}	0.5
2^{0}	1
2^{1}	2
2^{2}	4
2^{3}	8
2^{4}	16
2^{5}	32
2^{6}	64
2^{7}	128
2^{8}	256
2^{9}	512
2^{10}	1024

8-channel Multiplexer (inputs A_{7-0}, output Q

S2	S1	S0	Q
0	0	0	A_0
0	0	1	A_1
0	1	0	A_2
0	1	1	A_3
1	0	0	A_4
1	0	1	A_5
1	1	0	A_6
1	1	1	A_7

3-to-8 Line Decoder with Enable

A2	A1	A0	EN	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	0	0	0	0	0	1
0	0	1	1	0	0	0	0	0	0	1	0
0	1	0	1	0	0	0	0	0	1	0	0
0	1	1	1	0	0	0	0	1	0	0	0
1	0	0	1	0	0	0	1	0	0	0	0
1	0	1	1	0	0	1	0	0	0	0	0
1	1	0	1	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0
X	X	X	0	0	0	0	0	0	0	0	0

8-channel Demultiplexer (input A, outputs Q_{7-0})

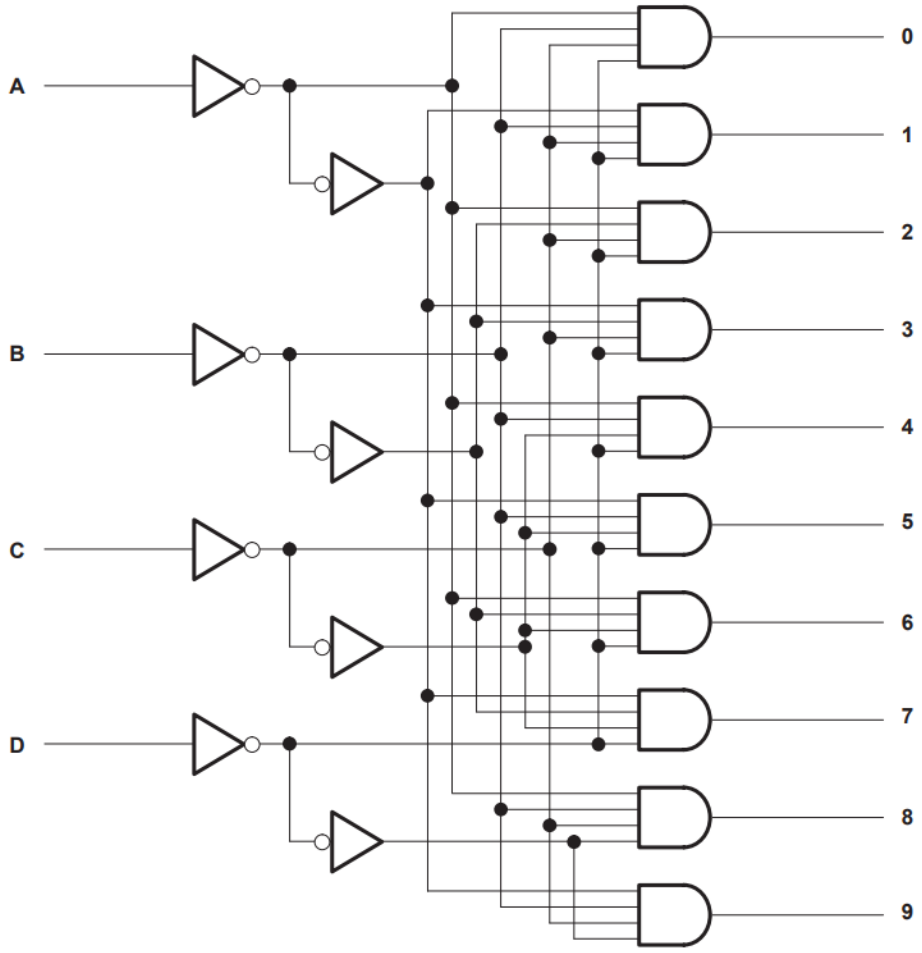
S2	S1	S0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0	0	0	0	0	0	0	0	0	0	A
0	0	1	0	0	0	0	0	0	A	0
0	1	0	0	0	0	0	0	A	0	0
0	1	1	0	0	0	0	A	0	0	0
1	0	0	0	0	0	A	0	0	0	0
1	0	1	0	0	A	0	0	0	0	0
1	1	0	0	A	0	0	0	0	0	0
1	1	1	A	0	0	0	0	0	0	0

8-to-3 Priority Encoder (Priority A7->A0)

A7	A6	A5	A4	A3	A2	A1	A0	E2	E1	E0	Ac
1	X	X	X	X	X	X	X	1	1	1	1
0	1	X	X	X	X	X	X	1	1	0	1
0	0	1	X	X	X	X	X	1	0	1	1
0	0	0	1	X	X	X	X	1	0	0	1
0	0	0	0	1	X	X	X	0	1	1	1
0	0	0	0	0	1	X	X	0	1	0	1
0	0	0	0	0	0	1	X	0	0	1	1
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0

Problem 1 (32 points)

Below is a (slightly modified) excerpt from a 74HC42 chip – a 4-to-10 line decoder. Although 4-to-16 is more traditional, 10 is a common number, and this fits nicely into a standard 16-pin chip (4 inputs + 10 outputs + power + ground).

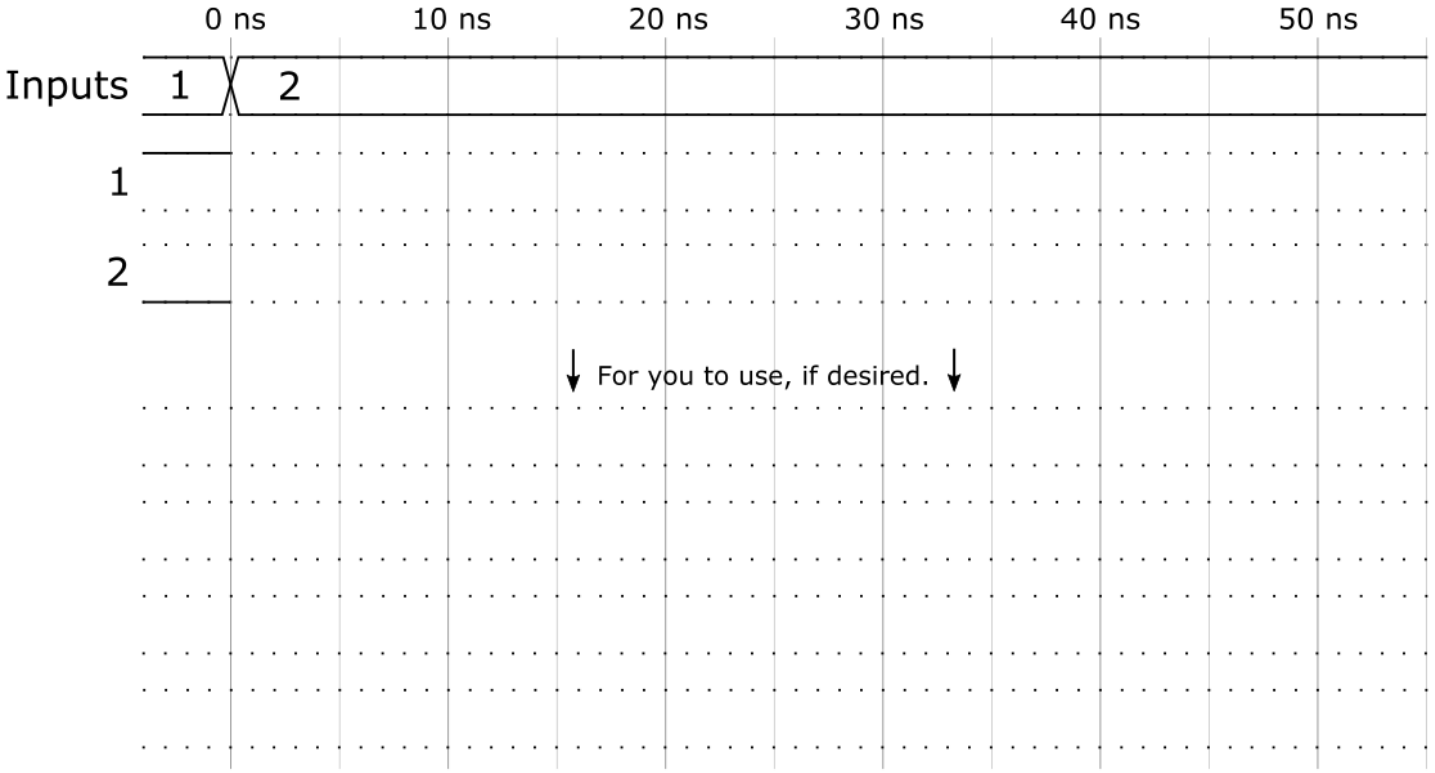


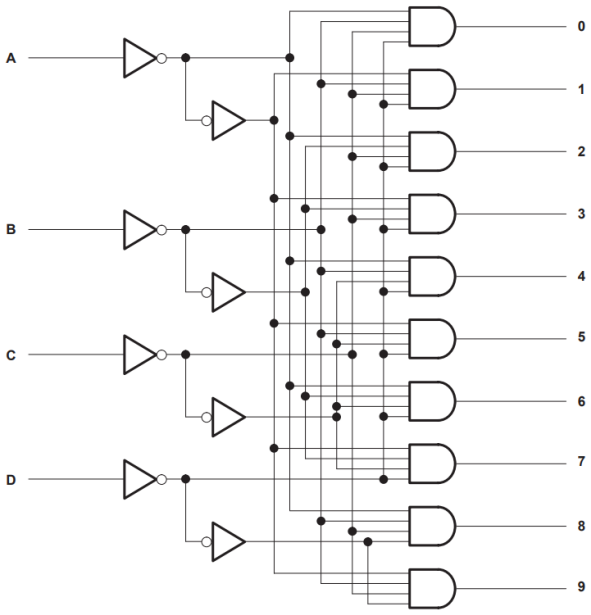
a) If the inputs (A, B, C, and D) are interpreted as a binary number, which one would be considered the least-significant (as related to the output numbering)?

b) Which output(s) will be high if all of the inputs are high?

c) If the propagation delay through an inverter is 8 ns and the propagation delay through a 4-input AND gate is 24 ns, what is the worst-case delay from any input to any output? In other words, if you change all of the inputs, how long do you have to wait before all of the outputs are correct?

d) Complete the following timing diagram for outputs 1 and 2 after the inputs switch from “1” to “2”; in other words, the inputs change from “0001” to “0010” at t = 0 ns. Output 1 is currently high, and eventually output 2 should be high. Extra space is provided at the bottom in case you want to sketch additional signals, and an extra copy of the schematic is below for your reference. Use the 8 ns and 24 ns delays from above.





Problem 2 (25 points)

Provide the decimal equivalent if these binary numbers are interpreted as unsigned, sign-magnitude, 2's complement, and fixed-point numbers in the specified format.

	unsigned	sign-magnitude	2's complement	unsigned fixed-point (NN.NN)
0100				
1011				
1100				

Perform the following conversions to hexadecimal.

1010_2 = _____$_{16}$

11010_2 = _____$_{16}$

0000111101011010_2 = _____$_{16}$

Perform the following unsigned operations. Restrict the result to 5 bits, and indicate if overflow occurred.

```
 01101          01101
+10001         +10100
```

overflow? y / n

overflow? y / n

Perform the following 2's complement operations. Restrict the result to 5 bits, and indicate if overflow occurred.

```
 10001          01101
+11101         -10100
```

overflow? y / n

overflow? y / n

Perform the following sign-magnitude operation. Restrict the result to 5 bits, and indicate if overflow occurred.

```
 01101
+10001
```

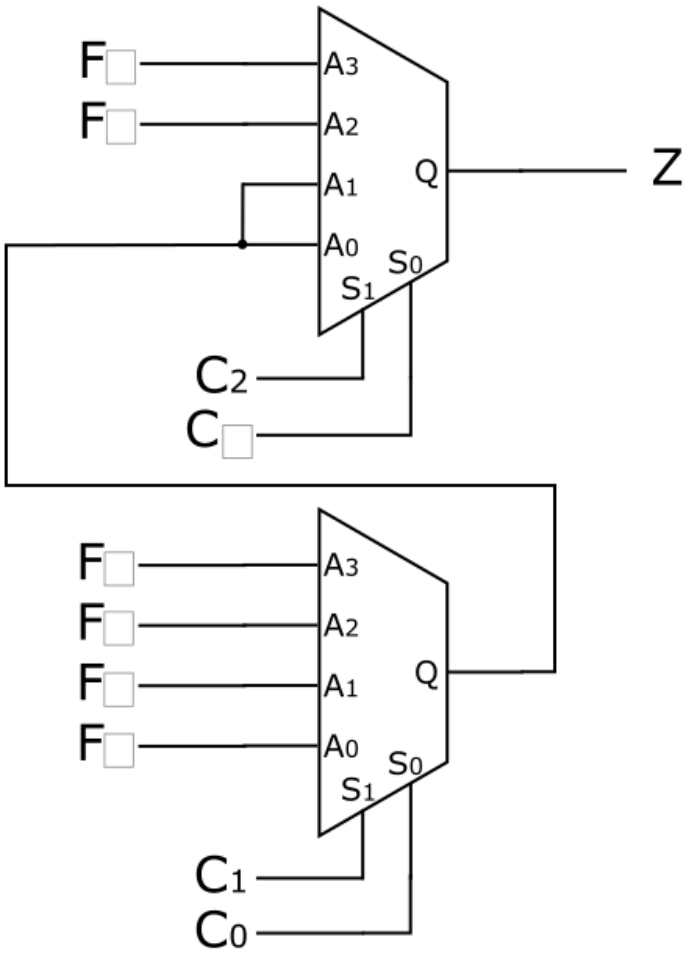
overflow? y / n

Problem 3 (24 points)

a) Consider two 8-to-3 priority encoders, each with inputs $A_{7\text{-}0}$ and outputs $E_{2\text{-}0}$, but with opposite priority: in one, A_7 has the highest priority and A_0 has the lowest, and in the other, A_0 is highest and A_7 is lowest.
Provide a set of input values (1s and 0s) that would result in the *same* output from both encoders, and one that would result in *different* outputs from each encoder. There are many correct answers here; you only need to provide one for each case.

These inputs will result in the same output from both encoders:	These inputs will result in different outputs from the encoders:
A_7 =	A_7 =
A_6 =	A_6 =
A_5 =	A_5 =
A_4 =	A_4 =
A_3 =	A_3 =
A_2 =	A_2 =
A_1 =	A_1 =
A_0 =	A_0 =

b) The goal of the circuit below is to multiplex six signals (F_5-F_0) onto signal Z based on the three control signals C_2-C_0. Complete the design by filling in the grey boxes. You need to choose the one remaining control signal, and you need to number the F signals appropriately (so that they make sense based on the control signals).



Problem 4 (18 points)

Fill in the result of the specified shifts.

	1 0 1 1 0 1 0 1
Logical shift right by 2	

	1 0 1 1 0 1 0 1
Logical shift left by 2	

	1 0 1 1 0 1 0 1
Arithmetic shift right by 2	

	1 0 1 1 0 1 0 1
Arithmetic shift left by 2	

	1 0 1 1 0 1 0 1
Barrel shift left by 2	

	1 0 1 1 0 1 0 1
Barrel shift right by 2	