ECE2020 A Fall 2018 Test 1

Name: _____

- Only a writing implement may be used on this exam (i.e. no books, notes, or any electronics).
- If the meaning of any question is not clear, please ask for clarification.
- Partial credit can only be awarded for work shown.

Honor pledge:

On my honor, I pledge that I will neither receive nor provide improper assistance in the completion of this test. I understand and accept my responsibility as a member of the Georgia Tech Community to uphold the Honor Code at all times, and I know that I have options for reporting honor violations at osi.gatech.edu.

GTID: _____ Signature: _____

Boolean Identities

Identity	$A + 0 = A$	$A \cdot 1 = A$
Dominance	$A + 1 = 1$	$A \cdot 0 = 0$
Idempotence	$A + A = A$	$A \cdot A = A$
Inverse	$A + \overline{A} = 1$	$A \cdot \overline{A} = 0$
Commutative	$A + B = B + A$	$A \cdot B = B \cdot A$
Associative	$A + (B + C) = (A + B) + C$	$A \cdot (B \cdot C) = (A \cdot B) \cdot C$
Distributive	$A \cdot (B + C) = A \cdot B + A \cdot C$	$A + B \cdot C = (A + B) \cdot (A + C)$
Absorption	$A \cdot (A + B) = A$	$A + A \cdot B = A$
DeMorgan's	$\overline{(A + B)} = \overline{A} \cdot \overline{B}$	$\overline{(A \cdot B)} = \overline{A} + \overline{B}$
Double Complement	$\bar{\bar{A}} = A$	
FOIL	$(A + B) \cdot (C + D) = A \cdot C + A \cdot D + B \cdot C + B \cdot D$	
Disappearing opposite	$A + \overline{A} \cdot B = A + B$	

This page is for scratch work and will not be graded unless you tell me that something on here needs to be graded.

0	0	0	0	
0	0	0	1	
0	0	1	0	
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0	1	1	0	
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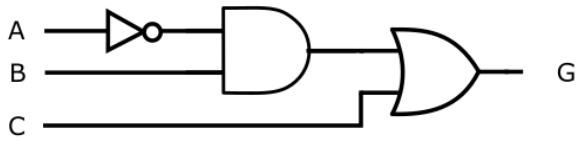
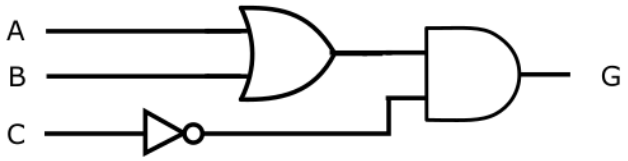
1	1	0	1	
1	1	1	0	
1	1	1	1	

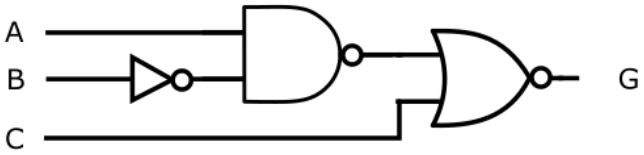
Problem 1: (20 points)
Write a Boolean expression for each of these gate schematics.



G = _____



G = _____



G = _____

Problem 2: (10 points)
A design team created the following logic expression for a project:

$$X = \overline{\overline{A + B \cdot C} + A \cdot D \cdot \overline{E}} + F \cdot G$$

That logic is correct, but at the last minute, the customer added a new requirement:
"Add a new input H. If H is low, output X must be low, otherwise use the same logic as before"
Make the simplest change possible to add the required behavior. You're welcome to either write a new expression, or just describe what you would do.

Problem 3: (25 points)

Implement the following Boolean expression in proper CMOS (N-FETs and P-FETs). Assume that inputs and their complements are available (i.e. you may use something like $\overline{C}$ as an input to a FET if needed).

$$F = \overline{(\overline{A} \bullet (\overline{B} + C))} + D$$

Derive expressions for the pull-up and pull-down switch networks (p.u. and p.d.) here:

p.u. = _____

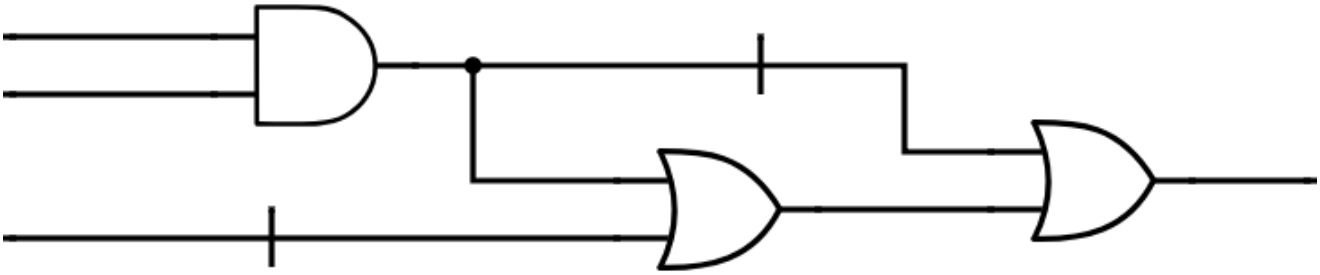
p.d. = _____

Draw CMOS here:

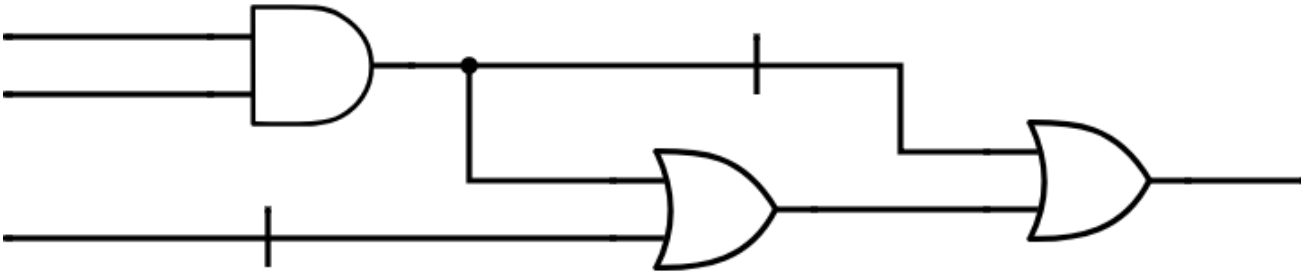
Problem 4: (20 points)

Manipulate the following mixed-logic schematic to implement it using only **ANDs** and **inverters**.

The same circuit is repeated here twice in case you ruin one. Please mark the one that you want graded.



⌂ Mark here if you want this one graded.



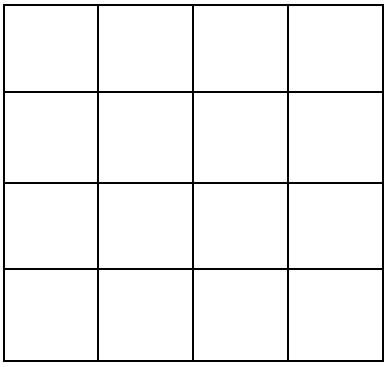
⌂ Mark here if you want this one graded.

Problem 5: (25 points)

Using the truth table below, create a K-map and solve for a minimal sum-of-products expression.

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Label the rows and columns of the K-map appropriately.



Y = _____