ECE 2020

Digital Systems Design

Quiz III

November 8, 2012

This exam is closed book and closed note and no calculators.

There are four questions. Do read them over before you start to work. If you need to make any assumptions, state them.

The meaning of each question should be clear, but if something does not make any sense to you, please ask for clarification. If you run out of room, please continue on the back of the previous page.

Good Luck!

Name (Please print)_____

This exam will be conducted according to the Georgia Tech Honor Code. I pledge to neither give nor receive unauthorized assistance on this exam and to abide by all provisions of the Honor Code.

Signed_____

Question	Score	Max
1		20
2		30
3		20
4		30
Total		100

1. (20) Floating point

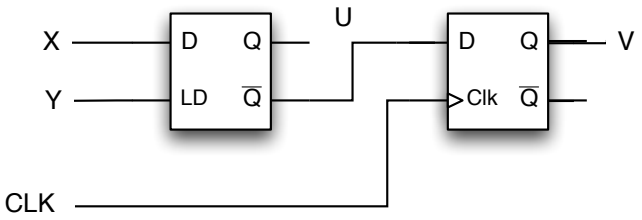
   a) Convert -28.375 to IEEE single precision floating point format. Your answer must be represented in hex.

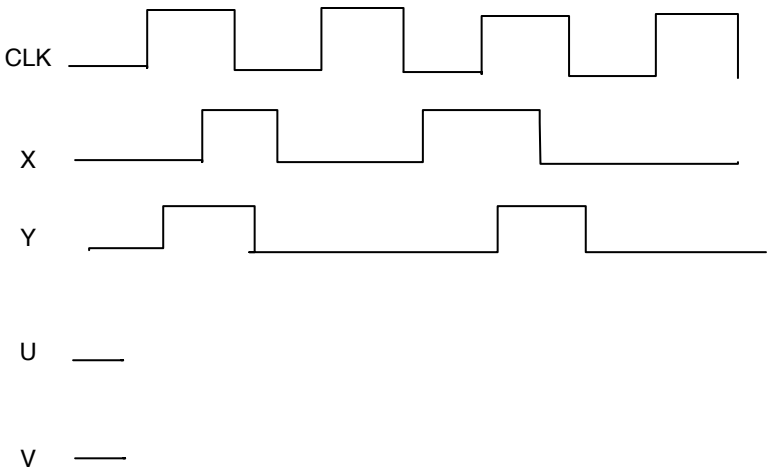
   b) Consider two IEEE single precision floating point numbers x = 0xACD2F739 and y = 0xACD2A739. Which number (x or y) is larger in magnitude?

2. 30) State holding elements

(a) (15) Design a positive edge triggered T-FF from D-latches, and any additional gates that are needed. (hint: you may wish to design a D-FF with the D-latches first).

(b) (15) For the given circuit (D Latch and negative edge triggered T-FF), complete the timing diagram. Note that U and V are initially 0.





3. (20) Counters. Design a synchronous mod 12 up counter that counts up mod 12 when cnt_en is asserted. You **must** use T flip flops and (a minimum number of) **any** other gates you need. Non-minimized (detection) circuits will not receive full credit.

4. (30) State Machines

   c) (15) Write a state diagram for a Mealy type state machine that detects all overlapping sequences 11011.

d) (15) Given the following symbolic state state table with input X and output Y, produce a state transition table and find minimized next state and output equations for Q_1^+ and Y only. Use the state assignment where the binary representation ($Q_2Q_1Q_0$) of state variables for state Si = i. You do NOT need to draw a schematic.

State	Input	Next State	Output
S0	0	S0	0
	1	S4	0
S1	0	S0	0
	1	S5	0
S2	0	S4	1
	1	S3	1
S3	0	S2	1
	1	S3	1
S4	0	S1	0
	1	S5	1
S5	0	S5	0
	1	S2	1