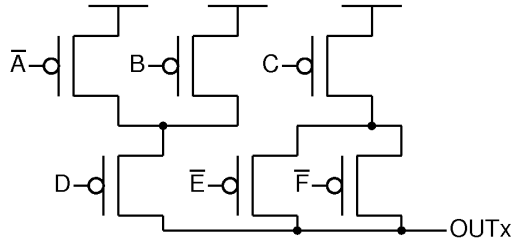
Instructions: This is a closed book, closed note exam. Calculators are not permitted. If you have a question, raise your hand and I will come to you. Please work the exam in pencil and do not separate the pages of the exam. For maximum credit, show your work.
Good Luck!

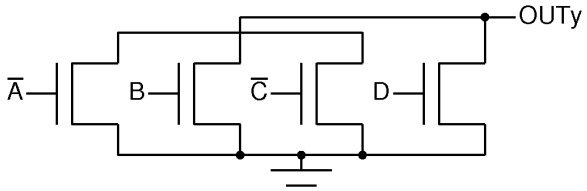
Your Name (***please print***) _____

1	2	3	4	total
30	20	26	24	100

Problem 1 (3 parts, 30 points) Incomplete Circuits

The three parts below contain (A) a pull up network, (B) a pull down network, and (C) an expression to be implemented. For (A) and (B), complete the missing complementary switching networks so the circuit contains no floats or shorts and write the Boolean expression computed by the completed circuit. For (C), design the entire switching network. Assume the inputs and their complements are available.





OUTx =

OUTy =

OUTz = $\overline{A}\cdot(B+\overline{C})\cdot(D+\overline{E}+\overline{F})$

Problem 2 (2 parts, 20 points) Boolean Algebra

Part A (12 points) Transform each of the following Boolean expressions to a form where they are ready for switch level implementation (i.e., there should only be bars over input variables, not over operations). The behavior of the expression should remain unchanged. **Do not implement**.

$OUT_X = \overline{\overline{A} \cdot B + C \cdot \overline{D}}$

$OUT_Y = \overline{\overline{A} \cdot \overline{B + C} \cdot \overline{D + E}}$

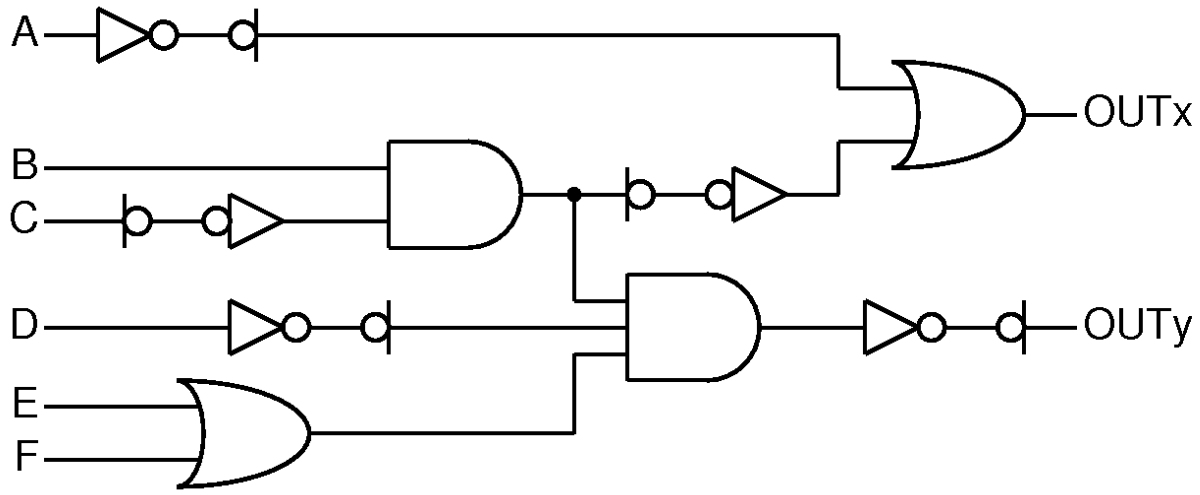
Part B (8 points) Derive the behavior of the following canonical product of sums (using maxterms) expression and complete the truth table.

A	B	C	$F_{(A,B,C)}$
0	0	0	
1	0	0	
0	1	0	
1	1	0	
0	0	1	
1	0	1	
0	1	1	
1	1	1	

$POS_{(MAXTERMS)} = (A + \overline{B} + C) \cdot (\overline{A} + \overline{B} + C) \cdot (A + B + C)$

Problem 3 (3 parts, 26 points) Mixed Logic Design

Part A (12 points) The following design has no supporting documentation. Derive the desired Boolean expressions and the implementation cost (in CMOS transistors).



OUT_X = _____

OUT_Y = _____

transistors = _____

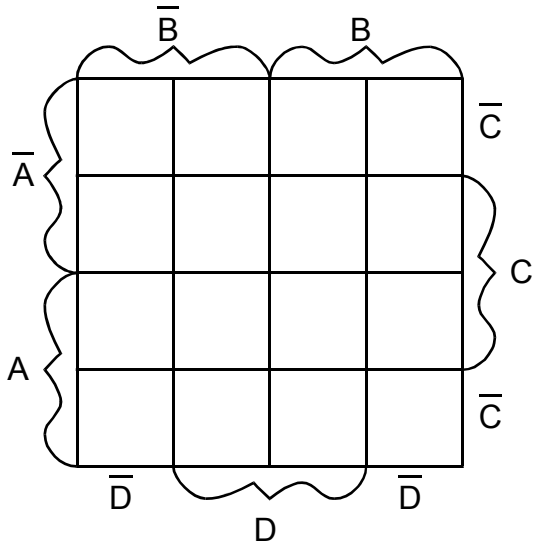
Part B (14 points) Now reimplement this expressions using NAND and NOR gates and inverters to minimize implementation cost. Use proper mixed logic notation. *Do not modify the expressions being implemented*. Determine the cost of this implementation (in transistors).

transistors = _____

Problem 4 (3 parts, 24 points) Karnaugh Maps

Part A (12 points) For the follow expression, derive a simplified ***sum of products*** expression using a Karnaugh Map. Circle and list *all* prime implicants, indicating which are essential.

$$Out = (A + B + D) \cdot (\overline{B} + \overline{C} + \overline{D}) \cdot (\overline{A} + C + D) \cdot (A + \overline{B} + C + D)$$

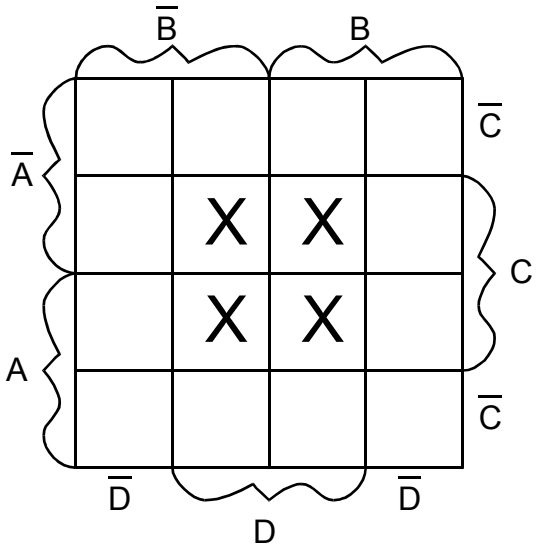


prime implicants	essential? yes	no
	☐	☐
	☐	☐
	☐	☐
	☐	☐
	☐	☐
	☐	☐
	☐	☐
	☐	☐

simplified **SOP** expression _____

Part A (12 points) For the follow expression, derive a simplified ***product of sums*** expression using a Karnaugh Map. The output is X when both C and D are high. Circle and list all prime implicants, indicating which are essential.

$$Out = A \cdot \overline{B} \cdot \overline{D} + B \cdot C \cdot \overline{D} + A \cdot B \cdot \overline{C} + B \cdot \overline{C} \cdot D$$



prime implicants	essential? yes	no
	☐	☐
	☐	☐
	☐	☐
	☐	☐
	☐	☐
	☐	☐
	☐	☐
	☐	☐

simplified POS expression _____