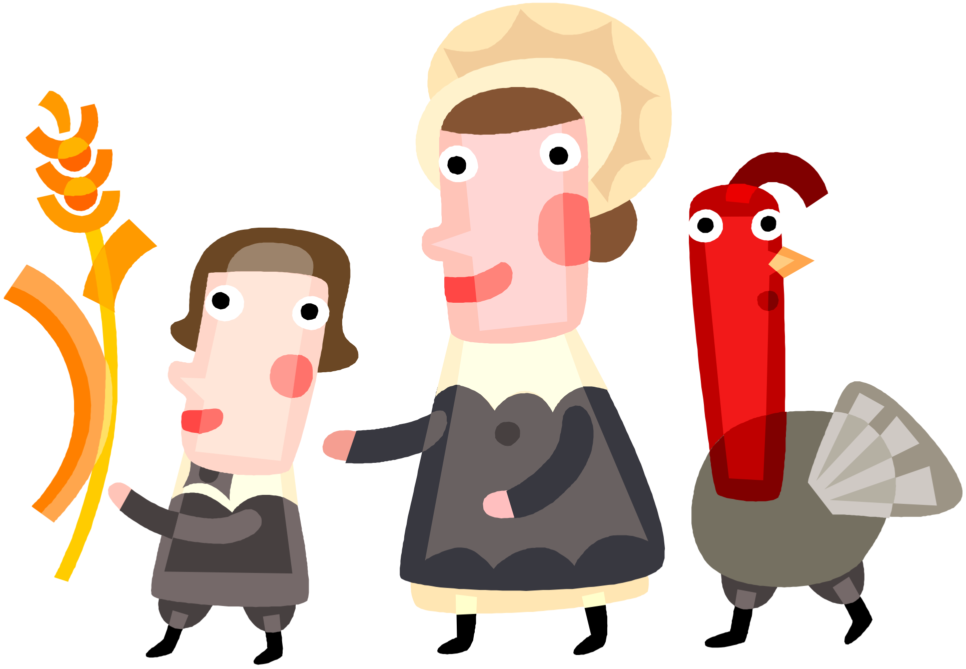
ECE 2030 12:00pm	Computer Engineering	Fall 2008
4 problems, 6 pages	Exam Three	21 November 2008

Instructions: This is a closed book, closed note exam. Calculators are not permitted. If you have a question, raise your hand and I will come to you. Please work the exam in pencil and do not separate the pages of the exam. For maximum credit, show your work.
Good Luck!

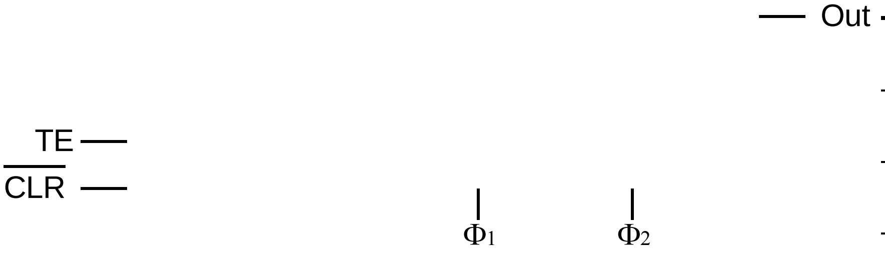
Your Name (***please print***) ____

1	2	3	4	total
22	30	22	26	100



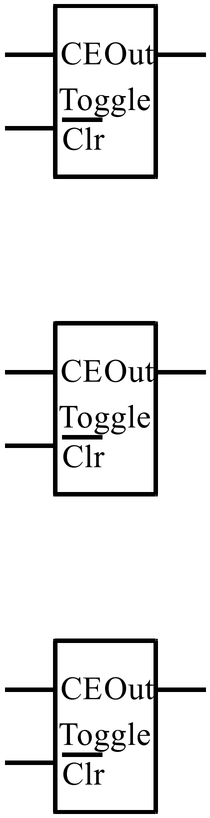
Problem 1 (2 parts, 22 points) Counters

Part A (10 points) Design a toggle cell using two transparent latches, two 2 to 1 muxes, and one inverter. Your toggle cell should have an active high toggle enable input **TE**, and an active low clear input **-Clear**, clock inputs Φ_1 and Φ_2, and an output **Out**. The **-Clear** signal has precedence over **TE**. Label all signals. Also complete the behavior table for the toggle cell.



TE	-Clear	CLK	Out
0	0	↑↓	
1	0	↑↓	
0	1	↑↓	
1	1	↑↓	

Part B (12 points) Now combine these toggle cells to build a **divide by six** counter. Your counter should have an external clear, external count enable, and three count outputs O_2, O_1, O_0. Use any basic gates (AND, OR, NAND, NOR, & NOT) you require. Assume clock inputs to the toggle cells are already connected. Your design must support multi-digit systems.



Problem 2 (3 parts, 30 points) Memory Systems

Part A (12 points) Consider a **256 Mbit** DRAM chip organized as **32 million addresses** of **eight bit words**. Assume both the DRAM cell and the DRAM chip are square. The column number and offset concatenate to form the memory address. Using the organization approach discussed in class, answer the following questions about the chip. *Express all answers in decimal (not powers of two).*

number of columns ____________________

number of words per column ____________________

column decoder required (*n* to *m*) ____________________

type of mux required (*n* to *m*) ____________________

number of address lines in column number ____________________

number of address lines in column offset ____________________

Part B (10 points) Consider a **one gigabyte** memory system with **128 million addresses** of **8 byte words** using a **32 million** address by **8 bit word** memory DRAM chip.

word address lines for memory system ____________________

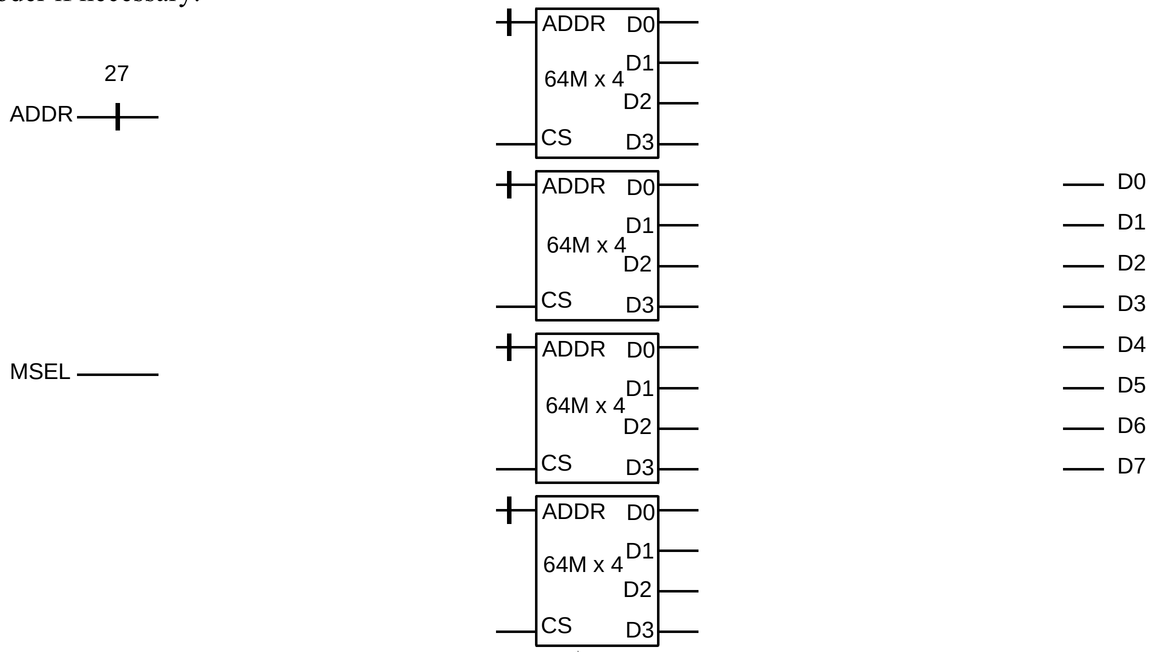
chips needed in one bank ____________________

banks for memory system ____________________

memory decoder required (*n* to *m*) ____________________

DRAM chips required ____________________

Part C (8 points) Design a 128 million address by 8 bit memory system with four 64M x 4 memory chips. *Label all busses and indicate bit width.* Assume R/W is connected and not shown here. Use a bank decoder if necessary.



Problem 3 (3 parts, 22 points) Datapath Elements and Instruction Formats

Part A (6 points) Suppose the following inputs (in `hexadecimal`) are applied to the 32-bit barrel shifter used in the datapath. Determine the output (in `hexadecimal`). Assume the shift amount (given in `hexadecimal`) is drawn from the 16-bit immediate value.

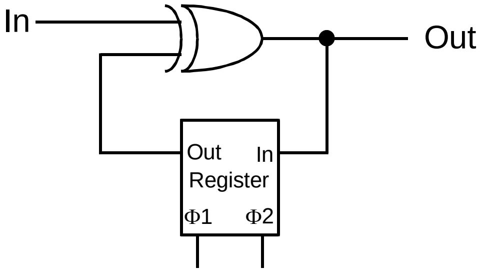
Shift Type	Shift Amount	Input Value	Output Value
logical	FFF0	12345678	
arithmetic	0014	A1024562	
rotate[1]	000C	F4A11BEE	

Part B (8 points) For each bitwise logical function specification below, determine the LF code (in hexadecimal) to correctly program the logical unit.

X Y	Out
0 0	LF_0
1 0	LF_1
0 1	LF_2
1 1	LF_3

logical function	LF
$\overline{X \oplus Y}$	
$X \cdot \overline{Y}$	
$X + Y$	
1	

Part C (8 points) For the state machine below, determine the output given the input and current register output for that cycle. Assume the register output is 0 (low) during the first cycle.



cycle	1	2	3	4	5	6	7	8	9
In	0	1	1	1	0	1	0	1	1
Out									

[1] Solution suggested by the National Turkey Association.

Problem 4 (2 parts, 26 points) Microcode

Using the supplied datapath, write microcode fragments to accomplish the following procedures. Express all values in hexadecimal notation. Use ‘X’ when a value is don’t cared. For maximum credit, complete the description field.

Part A (13 points) $R_4 = \frac{R_1 - (R_2 \times 5)}{2} - R_3$ **Use only R$_1$-R$_4$; modify only R$_4$.**

#	*X*	*Y*	*Z*	*rwe*	*im en*	*im va*	*au en*	*-a /s*	*lu en*	*lf*	*su en*	*st*	*description*
1													
2													
3													
4													
5													
6													
7													

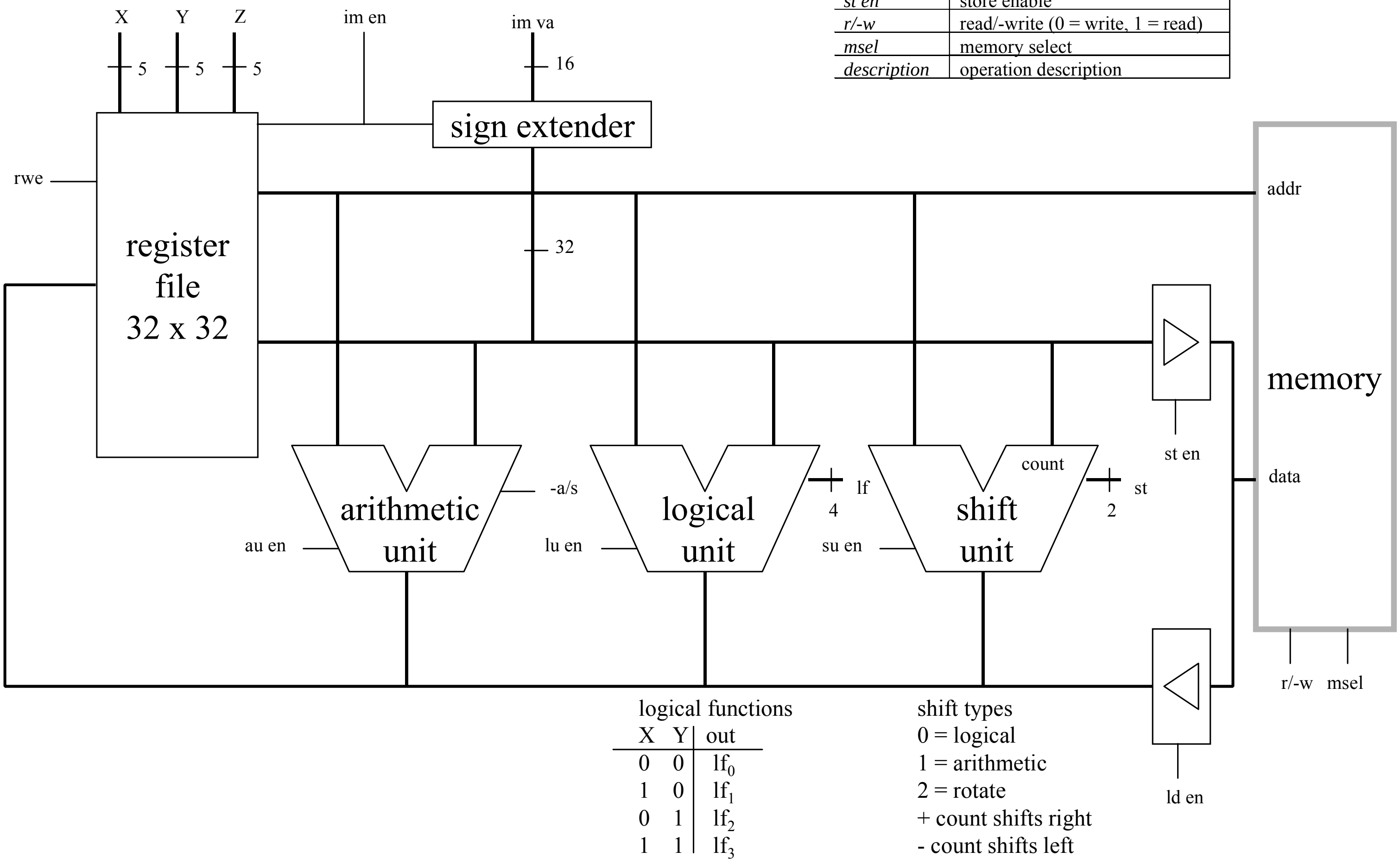
Part B (13 points) Write a microcode sequence that sums three packed ten bit values red, green, and blue of R$_1$ (format shown below). Assume the most significant two bits of the register are zero. Place the sum of the unpacked red, green, and blue values in R$_2$. **Use only R$_1$, R$_2$, and R$_3$; modify only R$_2$ and R$_3$.**

0	0	red	blue	green
31	30	29 20	19 10	9 0

#	*X*	*Y*	*Z*	*rwe*	*im en*	*im va*	*au en*	*-a /s*	*lu en*	*lf*	*su en*	*st*	*description*
1													
2													
3													
4													
5													
6													
7													
8													

cycle	cycle number
X	register driven onto X bus
Y	register driven onto Y bus
Z	register written from Z bus
rwe	register write enable
im en	immediate enable on Y bus
im va	immediate value

au en	arithmetic unit enable
-a/s	-add / sub (0 = add, 1 = subtract)
lu en	logical unit enable
lf	logical function
su en	shift unit enable
st	shift type
ld en	load enable
st en	store enable
r/-w	read/-write (0 = write, 1 = read)
msel	memory select
description	operation description



logical functions

X	Y	out
0	0	lf_0
1	0	lf_1
0	1	lf_2
1	1	lf_3

shift types
0 = logical
1 = arithmetic
2 = rotate
+ count shifts right
- count shifts left